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Hitachi, Ltd.

3-dimensional structure SRAM cell prototype
- Memory cell size reduced to 1/3 -

Hitachi, Ltd. (TSE:6501, NYSE:HIT) , in cooperation with Renesas Technology Corp. (Renesas Technology; Chairman & CEO: Dr. NAGASAWA Koichi) have developed a new three-dimensional (3D) structure SRAM (Static Random Access Memory) cell, and successfully confirmed its operation. The 3D-structure SRAM consists of four transistors, two of which are vertical poly-silicon MOS transistors formed above the normal transistors. By employing this 3D-structure, it was possible to reduce the surface area of the memory cell to one-third conventional size. This technology is expected to become a fundamental structure for processes beyond the 45nm generation, and contribute to overcoming the barriers to higher integration in SRAM.

SRAM is widely used as an on-chip memory for SoCs and memory in cellular phones; as it has superior low power consumption features, and does not require a refresh operation for data retention. As mobile terminals, such as cellular phones, become even more functional, however, even higher density SRAM is required, as the amount of memory needed doubles with each progressive generation. As dimensions decrease further in response to such needs for higher integration, and for processes beyond-45nm process generation, it is expected however, that a limit will be reached whereon both standby current is controlled and stable operation maintained.

In response to this challenge, Hitachi together with Renesas Technology, successfully developed a 3D structure SRAM cell to realize compact high-density SRAM memory for beyond-45nm process generation.

Details of the 3D structure SRAM cell are as below:

(1) **Columnar vertical poly-silicon MOS Transistor :** A columnar poly-silicon MOS transistor stacked on the silicon substrate was developed. The source and drain of the transistor are located at the top and bottom of the cylinder respectively, and a surrounded gate structure was employed around the sides. One feature is that as the

sides serve as a channel, vertical current flow occurs, achieving 20μA and a large on-current compared to conventional poly-silicon transistors.

(2) **Four transistor SRAM cell** : The 3D-structure SRAM cell consists of four transistors; two standard transistors and two vertical transistors. As the vertical transistors are formed above the standard transistors, the cell area is equivalent to that of two transistors, enabling a significant decrease in area compared to conventional SRAM.

(3) **Dual-word-voltage scheme :** A scheme allowing the operating voltage of the word line to differ between the read and write operations. Stable read and write operations were achieved by controlling the reversal of data in the memory cell by current flow during read out.

(4) **Electric-field-relaxation scheme** : Technology achieving a cell leakage current of 88.7 fA/cell, a level equivalent to conventional SRAM cells, by optimizing the voltage applied on the memory cell during standby to control leak current.

The principle operation was proved through confirming successful read and write operations, in a prototype memory cell using 130nm CMOS process and the above circuit technologies. Further, the cell size of the prototype was found to be 0.78μm^2, one-third the size of conventional SRAM.

This technology will help overcome the barriers in achieving compact, high density, low cost SRAM for beyond-45nm process generation, and will support the further progress of mobile information terminals in the future.

These results were presented at the Symposium on VLSI Circuits, held in Hawaii, U.S.A. from 17th June 2004.

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