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Hitachi, Ltd.

Development of a four-transistor-type SRAM cell using double-gate FD-SOI transistor
- Reducing leakage current by $^{1}/_{1,000}$ and enabling embedding in SoC -

Tokyo, June 18, 2004 -- Hitachi, Ltd. (TSE:6501, NYSE:HIT) has designed a new small-area low-power SRAM cell, suitable for SoC (System-on-a-Chip) used in mobile devices, and has verified its effectiveness by simulation. The new SRAM cell is composed of four FD-SOI[*1] (Fully-Depleted Silicon-On-Insulator) transistors, with a double-gate structure. The standby leakage current is about $^{1}/_{1,000}$ compared to a conventional four-transistor memory cell. This technology enables a small-area high-density four-transistor SRAM cell to be embedded into a low-power SoC.

The increasing functionality of mobile information terminals and the expansion of its market, rely on the increasing performance of the SoC. Performance of a SoC is measured not only by its high operating speed but also by low power consumption; an important factor in determining battery life of mobile equipment. As many SRAM modules are employed as embedded memory in SoC, the performance and power consumption of the SRAM has a great impact on the performance of the entire SoC. As manufacturing dimensions decrease, however, it has become increasingly difficult to simultaneously achieve both high-speed operation and low power consumption due to factors such as increase in leakage current and process variations. As a result, various circuit techniques have been employed to overcome these problems in the 90-nm manufacturing process. At the same time, it has been pointed out that circuit technology alone will be insufficient for the 65-nm process generation, and that new technology, including new device structures, will need to be developed.

In response to this challenge, Hitachi CRL designed a new small-area low-power SRAM memory cell structure for SoC embedded memory, composed of four FD-SOI transistors.

Features of the new memory cell are as below:

(1) **Double-gate-type FD-SOI transistor:** An FD-SOI transistor, whose process variation and leakage current is lower than other SOI transistors, was used. In a conventional transistor, the drive current is controlled by changing only one gate-node potential. The drive current of this transistor is controlled by changing two gate-node potentials; this dual gate structure enabling good current controllability.

(2) **New feedback circuit in memory cell:** The new memory cell is composed of four transistors. In a conventional four-transistor memory cells, power consumption is an issue as standby leakage current is used to retain data and thus compared to a conventional six-transistor memory, power consumption is high. The new design controls transistor current and reduces standby leakage current using a new feedback circuit. This circuit is located within the memory cell, and controls the data retaining current in four steps using the double-gate structure. Thus current required for data retention is only directed to necessary current paths, and standby leakage current is drastically reduced.

Simulation was used to evaluate the four transistor memory cell. Compared to a conventional four-transistor memory cell, standby leakage current was decreased to $^{1}/_{1,000}$, and operating speed was 20% higher. These results indicate that this new four-transistor memory cell is applicable to SoC which requires low power operation. Further, when compared to a conventional six-transistor memory cell, the new feedback circuit developed also achieves a 20% increase in operating speed and $^{1}/_{20}$ leakage current. As four-transistor and six-transistor memory cells may simultaneously be integrated on the one LSI, depending on the performance requirements of the LSI, it is possible to select combinations of small-area high-density four-transistor memory cells and high-speed six-transistor memory cells, to improve the overall performance of the SoC.

These results were presented at the Symposium on VLSI Circuits, held in Hawaii, U.S.A. from 17th-19th June 2004.

■ **Technical Terms:**

(1) **FD-SOI**: Fully Depleted Silicon-on-Insulator. A transistor is formed in a SOI layer. The SOI layer is formed above an insulator layer, which is formed above a silicon substrate. In an FD-SOI transistor, the thickness of the SOI layer is less than 50 nm, and the channel region is fully depleted. In the FD-SOI transistor, the drive (On) current is high and the leakage (Off) current is low, and therefore the transistor performance is high.

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