High-speed DRAM circuit technology for the 1V generation

- Power consumption reduced to 1/3 with no loss in operation speed -

TOKYO, Japan, September 26, 2001 --- Hitachi, Ltd., (TSE: 6501) and Elpida Memory, Inc. today announced that they have developed "low-voltage high-speed sense amplifier circuit(*1) technology" which reduces power consumption to 1/3 the level of current DRAMs (Dynamic Random Access Memory). The technology developed overcomes the problem of loss in operation speed caused by the delay in signal amplification which occurs when DRAM voltage is decreased, and achieves the same operation speed with just 1V as for the current 1.8V. This result is expected to provide key technology in the next generation multi-gigabit DRAM where 1V voltage is required.

To attain a ubiquitous information society, large capacity, high-speed and low power devices are necessary for high-speed mobile terminals processing large volume data such as image and voice. Among such devices, multi-gigabit DRAM, expected to become a key device, needed low voltage technology to overcome the increase in power consumption that accompanies greater integration.

In DRAMs, however, as voltage decreases, signal (data) read from the memory cell(*2) to the sense amplifiers decreases, leading to a delay in the amplifying operation in the sense amplifier circuit, resulting in an overall decrease in DRAM operation speed. Thus, the development of new sense amplifier circuit technology that would allow high-speed amplification even at low voltages was required.

1. Cause of Speed Degradation: Sense amplifiers are connected to a number of other sense amplifiers through a common source line. When voltage is applied to the common source line, the first sense amplifier to which current flows, continues to receive priority in current flow, and the operation of the other sense amplifiers is deferred. Further, as time passes the amount of current flowing to the deferred sense amplifiers decreases, resulting in a decrease in overall DRAM operation speed. At the present 1.8V voltage level, there is sufficient current flow so as this effect is not clearly visible, however, when voltage levels are decreased to 1V, the drop in DRAM operating speed can no longer be ignored.

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2. Development of a low voltage high speed sense amplifier circuit: To overcome the disturbance from neighboring sense amplifiers, a source node which was previously shared by several sense amplifiers, was allocated to one sense amplifier. As a result, the current flowing through a single source node all flows to an individual sense amplifier, and no delay or difference occurs in operation start-up time of neighboring sense amplifier circuits.

Further as a result of using circuit simulation to evaluate this technology, equivalent speeds to a voltage of 1.8V were achieved. Thus, power consumption was decreased to 1/3 the level of operation at 1.8V. Furthermore, as this circuit design can incorporated into previous methods with no additional change, chip area increase is contained within 3%. This technology can be applied not only to standard high density DRAM but also to embedded DRAM arrays.

The above research achievement is scheduled to be presented at the International Conference on Solid State Devices and Materials (*SSDM)* to be held in Tokyo from 25th September 2001.

<Note>

(*1) Sense amplifier circuit: Circuit which amplifies read out signals

(*2) Memory cell: Memory unit which stores 1 bit of information

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