Development of High-performance Strained-Silicon-Transistor Technology
- 2.2-fold increase in electron mobility through improved surface planarization -

Tokyo Japan, December 6, 2001 - Hitachi, Ltd. (NYSE:HIT) has developed a technology to enhance the performance of strained-silicon (Si) transistors, which is expected to be used in the next generation CMOS (Complementary Metal-Oxide-Semiconductor) technologies. The strained-Si transistor is fabricated on a Si layer deposited on a substrate containing SiGe, and utilizing the resulting lattice distortion in Si to achieve high carrier mobility. As a result of planarizing the SiGe layer by chemical mechanical polishing (CMP), it was possible to minimize the performance degradation due to surface roughness, and achieved a 2.2-fold increase in mobility compared to conventional Si-MOS transistors. This result demonstrates the advantage of the strained-Si transistors over the Si transistors to realize ultrahigh-speed CMOS.

Until now, CMOS, a typical semiconductor device, has followed a paradigm of improving performance by decreasing dimensions and increasing the scale of integration. Beyond the so-called 100nm-generation, where following this paradigm is considered difficult, a new technology to improve performance not reliant only on downsizing, will be required. One candidate, which has recently been the center of interest, is strained silicon. It has been known that carrier mobility increases when the crystal lattice of Si is stretched. Thus if Si is placed on SiGe, which has a slightly wider lattice spacing than Si, then it is stretched (strained), and mobility is increased. A strained-Si transistor uses this strained layer as the channel layer (the layer through which electrons flow). Until now, however, although improvement in mobility has been confirmed, the breakthrough improvement in performance expected with the strained-Si transistor has not been realized.

Hitachi undertook the challenge of improving the performance of the strained-Si transistor. Hitachi found that if the surface of the SiGe layer was rough, so was the surface of the strained-Si layer, and this led to a decrease in carrier mobility.

Based on these findings, Hitachi developed the strained-Si technology of growing the strained-Si layer on a planarized Si-Ge layer surface to achieve full performance expected in strained-Si. Features of the technology are as follows:

(1) CMP[*1)] was introduced as a planarization process of the SiGe layer, and surface roughness was reduced to an atomic-level flatness of 0.4 nm.
(2) A chemical vapor deposition technique was developed to re-grow the strained-Si layer

after CMP on the planarized SiGe layer.

(3) The heat-treatment temperature was optimized to minimize performance degradation during the transistor fabrication process, due to diffusion of Ge from the SiGe layer to the strained-Si layer and strain relaxation of the strained-Si layer.

Using this technology, MOS transistors with a channel length of 0.24 μm were fabricated. Both electron and hole mobilities were found to have increased by +120% and 42% over the conventional Si transistors, respectively. The current drive was found to have significantly improved by, +70% for the n-channel, and 51% for the p-channel, over the conventional Si-MOS devices. This result shows that the strained-Si technology is indeed a viable candidate for next-generation high-speed CMOS technology.

<Technical Terms >

(*1) CMP: Chemical Mechanical Polishing. A technique to smoothen surfaces by polishing both chemically and mechanically using a slurry containing alkaline solution and polishing medium.