10th February 2003
Hitachi, Ltd.

Successful development of multi-processor low-power circuit technology
- Reducing power-consumption to one-third ($^1/_3$) & design/testing time to one-tenth ($^1/_{10}$) -

Hitachi, Ltd. (NYSE:HIT) has successfully developed the "autonomous decentralized universal controller", a new low power circuit technology for multiprocessors (a chip which integrates several microprocessors), the next-generation high performance device. The evaluation results from a prototype chip with this circuit, indicated $^1/_3$ multiprocessor power consumption, $^1/_{10}$ design time and $^1/_{10}$ performance testing time. This technology optimizes the processing speed to power consumption ratio, without placing additional burden on multiprocessor design or testing time.

In system LSIs, represented by microprocessors - the "brain" of PCs, increased performance has been achieved by consolidating complex functions on one chip, this itself being made possible by shrinking devices and higher integration. Further, for the next generation, chip multi-processor technology which integrates several processors on one chip, is being considered as a method for quickly achieving an increase in performance. However, as chip integration increases, increased power consumption becomes a problem. "Universal control technology", which optimizes the operating conditions (clock frequency, supply voltage, body bias) and eliminates unnecessary power consumption, is being proposed as a method of achieving low power consumption in processors. To apply this method to multiprocessors however, many problems such as the need for a special control in the circuit, increased design complexity and testing time, existed.

A new circuit technology, "autonomous decentralized universal control", was developed for multiprocessors to overcome such problems. Features of the technology developed are as follows:

(1) A "C-BIST (compound built-in self-test) circuit" was introduced to automatically measure the performance of each processor in the multiprocessor. Testing time was dramatically reduced due to this circuit.
(2) A "SI-LUT (self-instructed look-up table)" which records the performance data from the C-BIST circuit is deployed in each processor. This table measures the required performance and the amount of data to be processed; "learns" and decides on the optimal operating conditions (combination of clock frequency, supply voltage, body bias) to minimize power consumption based on data recorded in the table.
(3) Due to the technologies described above in (1) (2), it is possible for each processor to autonomously set the processing speed/power control, thus reducing the design time for the entire chip.

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When this technology was applied to a 32-bit arithmetic logic unit (ALU) with 100nm gate-length MOS transistors, power consumption was decreased to one-tenth of previous levels. For a multiprocessor with a 4-processor configuration, the estimated average-power reduction was to one-third of previous levels. Further, design hours and chip testing time were estimated to be one-tenth of that previously required. The significance of this technology will increase as the multiprocessor design becomes more common.

This technology was announced at the International Solid-State Circuits Conference (ISSCC), which was held from 9th February 2003, in San Francisco, California, U.S.A.

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