Semiconductor Process and Manufacturing Technologies for 90-nm Process Generation

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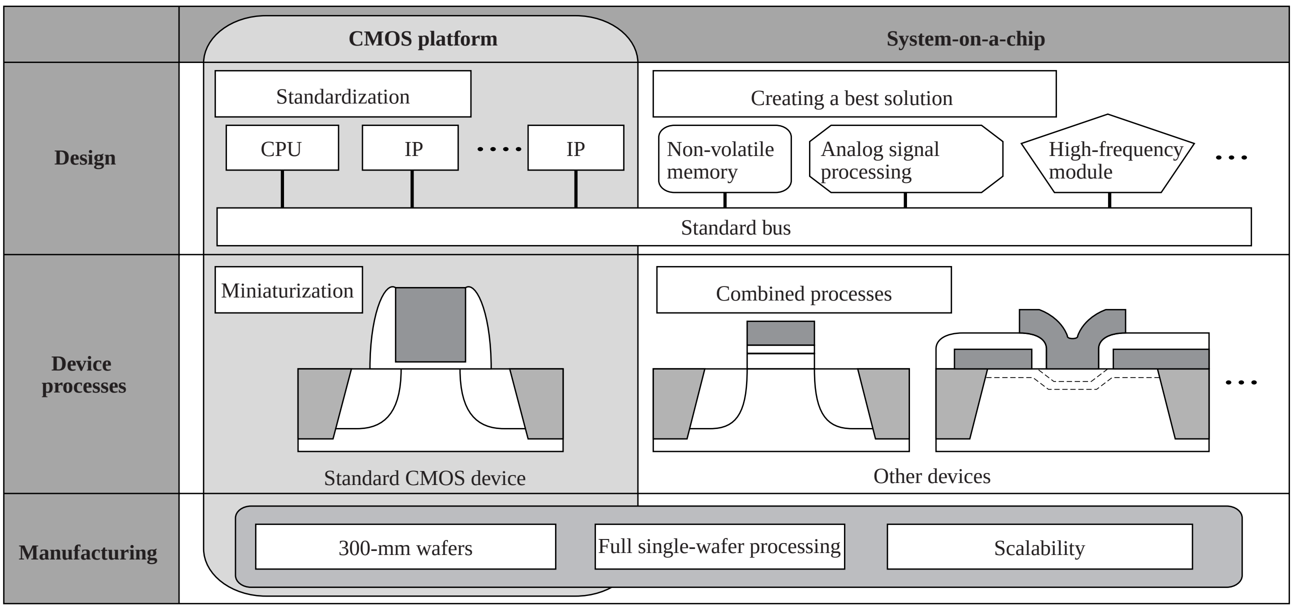
OVERVIEW: Hitachi is actively working on the miniaturization and standardization of CMOS (complementary metal-oxide semiconductor) devices and on the establishment of a CMOS platform. This will enable Hitachi to share IP (intellectual property), a design asset. Furthermore, in conjunction with this platform, Hitachi will develop core devices other than CMOS devices and combine rich IP to provide customers with system-on-a-chip products as an optimal solution. Hitachi is adopting an APC (advanced process control) technology to reduce variation in its process and manufacturing technologies. It also aims to support the production of a small volume of many products and to respond quickly to market and customer needs, especially through the full single-wafer processing line for 300-mm wafers at Trecenti Technologies, Inc. (TTI).

INTRODUCTION

IN the semiconductor industry, the miniaturization of semiconductor devices has enabled developing high-performance and low-cost products by increasing the number of logic circuits that can be integrated on an LSI (large-scale integration) and by raising the operating frequency. In this environment, the designer needs to develop large-scale, complex, and high-speed systems in a relatively short time, and sharing the IP is indispensable to making this work more efficient. Effective IP sharing requires that design rules and libraries be standardized, and to this end, Hitachi has been actively promoting the miniaturization and standardization of a CMOS platform in cooperation



CPU: central processing unit

Fig. 1 —"System-on-a-chip" as an Optimal Solution.
In the "System-on-a-chip" era, customers must be provided with system LSIs. This requires close interfacing among design, device processes, and manufacturing.

with Semiconductor Technology Academic Research Center (STARC) in Japan.

At the same time, Hitachi has been independently developing core devices other than CMOS devices and adding to IPs to provide customers with optimal system-on-a-chip products. For manufacturing the system-on-a-chip products, Hitachi is pursuing a production format centered about TTI, a company that has a full single wafer processing line for 300-mm wafers, to respond quickly to market and customer needs.

In this report, we focus on CMOS devices, whose standardization is progressing, and describe the manufacturing technologies for minimizing feature sizes with the aim of improving device performance. We examine, in particular, how variation in device characteristics increases relative to the variation in manufacturing technologies when shrinking feature sizes, and outline APC technology as a countermeasure to this problem.

MINIATURIZATION OF CMOS DEVICES

Achieving High Performance by Miniaturizing

A CMOS device is a switch that turns the current between the source and the drain on and off. The basic performance of this switch can be determined by examining whether a large drive current is made to flow when the switch is on and whether the leak current can be reduced when the switch is off.

The most effective way of obtaining a large drive current when the switch is on is to reduce the gate length and to make the gate insulation-film thinner [Fig. 2 (a)]. In other words, the drive current increases by reducing the distance covered by carriers in each channel and by increasing the number of carriers.

Carrier mobility is also known to be greatly affected by the stress applied to channels[1], and two key methods to improve mobility are now being studied. The first method controls the stress applied to the insulation film covering the device, and the second method grows a Si substrate on a SiGe crystal and applies strain to the Si layer.

Hitachi has successfully fabricated a prototype CMOS device with a 50-nm gate length[2] and one using a strained Si layer[3] [Fig. 2 (b) and (c)].

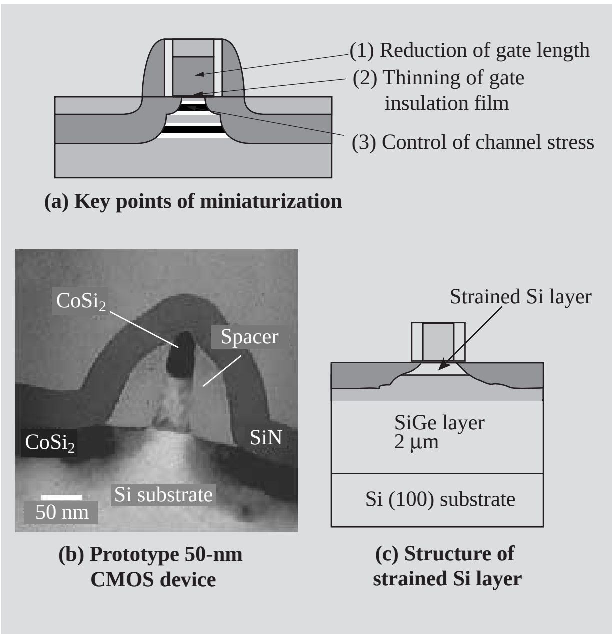


Fig. 2 —CMOS Device Miniaturization.
The basic performance of a CMOS device is determined by whether a large drive current is made to flow when the switch is on and whether leak current can be reduced when the switch is off.

Elemental Technologies for Miniaturization

(1) International Technology Roadmap for Semiconductors (ITRS) 2001 edition for CMOS devices

Table 1 shows the 2001 version of the ITRS for CMOS miniaturization. It describes the ongoing reduction of the gate dimensions and the thinning of the gate insulation film with the node size decreasing from 130 to 90 nm. Mass production of devices with 90-nm nodes is expected to start sometime in 2003 or 2004, and we are now aiming at establishing manufacturing technologies that can produce products

TABLE 1. ITRS: 2001 Edition for CMOS Devices
The 90-nm era is expected to begin sometime in 2003 or 2004.

Year	2001	2002	2003	2004
Technology node (nm)	130	115	100	90
Gate dimensions (nm)	65	53	45	37
Gate-dimension accuracy (3σ) (nm)	6.31	5.30	4.46	3.75
Gate insulation-film thickness (EOT)(nm)	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4
Wiring pitch (nm) bottom layer	350	295	245	210
Wiring pitch (nm) intermediate layer	450	380	320	265
Permittivity (k) of inter-layer insulation film	3.0–3.7	3.0–3.7	2.9–3.5	2.5–3.0

EOT: effective oxide thickness
[International Technology Roadmap for Semiconductors (ITRS) : 2001 Edition]

with gate dimensions under 50 nm and an insulation film thinner than 1.0 nm.

(2) Fine-processing technologies

The core technologies behind fine processing are lithography and dry etching. In lithography, the resolution can be improved by shortening the wavelength of the light source in the exposure equipment and by increasing the NA (numerical aperture) of the lens. For 90-nm nodes, the plan is to adopt an ArF light source (wavelength: 193 nm) and a lens with an NA of 0.75 or greater. The development of resist material for ArF use is also progressing and stabilizing and resolving a 90-nm resist pattern has already become possible. Our future goal is to develop a lens with an NA of 0.8 and resist material that is highly resistant to dry etching.

Also, while phase shifting and OPC (optical proximity correction) are becoming indispensable techniques for raising the resolution performance, the increase in mask-drawing data has resulted in a dramatic jump in mask costs. Consequently, drastic measures in manufacturing processes and equipment that can significantly decrease mask cost are strongly anticipated.

In dry etching technology, a “slimming process” for reducing the resist dimensions has become necessary considering that the target gate length takes on dimensions less than the resolution of the exposure equipment[4]. The gate-electrode material should now contain SiGe polycrystal to reduce depletion, and it is necessary to achieve a rectangular cross-sectional shape without causing dimensional shifts. Furthermore, obtaining a highly accurate impurity-concentration distribution in a CMOS device now requires accurate processing in the sidewall spacers.

(3) Gate insulation-film technology

Because the thickness of the gate insulation films will decrease to 1.0 nm or less in 90-nm CMOS devices as shown in Table 1, the tunnel current, which is one leak-current component when the switch is off, will flow through the gate insulation film, which is problematic. To decrease this tunnel current, the use of high dielectric constant film instead of silicon-oxide film is now being studied. This alternative has not been fully adopted yet, however, as good electrical characteristics cannot be ensured at the interface between Si and the high dielectric constant film. For this reason, we are developing plasma nitridation that can improve controlling the nitrogen concentration distribution in the nitridation of conventional silicon-oxide film. This way we hope to decrease the leak current while achieving good electrical characteristics at the interface between Si and nitrided silicon-oxide film.

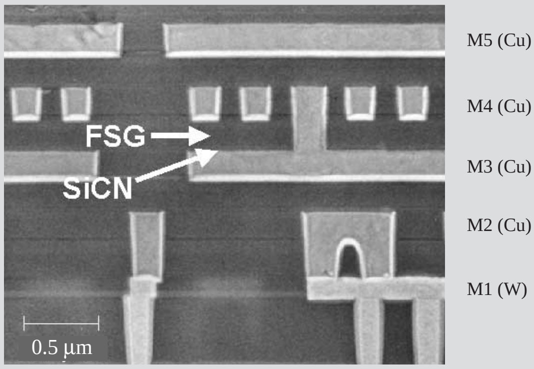


Fig. 3 —Cross Section of 0.36-µm-pitch Cu Wiring.
Hitachi uses Cu wiring with a 0.36-µm pitch for a 130-nm-node CMOS, as well as fluorine-doped silicon oxide as an inter-layer film and SiCN as a Cu-barrier film to reduce permittivity.

(4) Cu wiring technology

Reducing the wiring resistance and the inter-layer film capacitance is crucial to propagating the high-speed pulses generated in a CMOS device with little delay and waveform distortion. Hitachi has been using Cu wiring with a 0.36-µm pitch for a 130-nm-node CMOS and has reduced effective dielectric constant to as far as 3.7 by using fluorine-doped silicon-oxide film as an inter-layer film and SiCN as a Cu-barrier film, as shown in Fig. 3[5].

According to the ITRS shown on page 91, the Cu-wiring pitch will decrease even more to 265 nm or less in the near future. This, however, will allow coverage to deteriorate in the CU-filling process of the damascene technique, as well as voids to occur and resistivity to increase. We therefore need to change the conventional approach of combining plating with sputter technologies to combining plating with CVD (chemical vapor deposition) technologies.

The dielectric constant of the inter-layer isolation-film material has so far been reduced from approximately 4.2 for silicon-oxide film to approximately 3.7 for fluorine-doped silicon-oxide film. The adoption of CVD film and coating film is progressing, however, as future dielectric constant targets are at 3 or less. Inter-layer films have other requirements in addition to those associated with

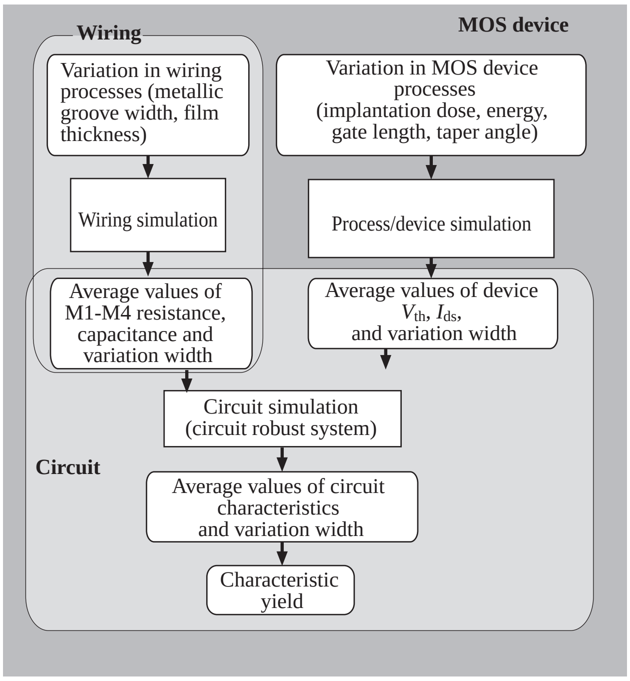
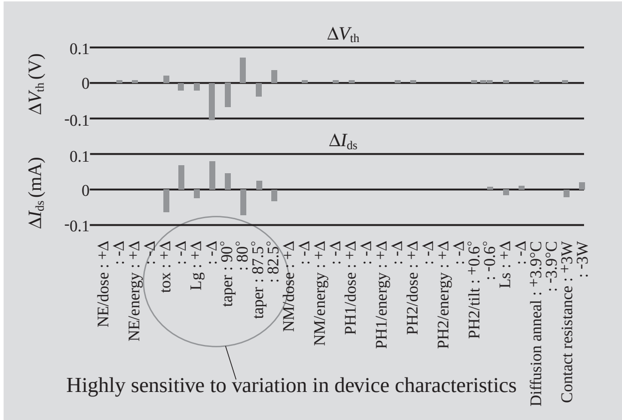


Fig. 4 —Raising Robustness of Circuits and Devices at Development Stage.
Manufacturing variation for each elemental process is analyzed in circuit simulations and device models to make early improvements to circuits and devices and to raise their robustness.



ΔI_{ds} : variation in drive current (I_{ds})
ΔV_{th} : variation in threshold voltage (V_{th})

Fig. 5 —Sensitivity of Drive-current (I_{ds}) and Threshold-voltage (V_{th}) Variation.
Drive current and threshold voltage are highly sensitive to variation in gate length, gate insulation-film thickness, and gate-electrode taper angle.

dielectric constant. For example, Cu filling should not be obstructed by degassing, cohesiveness with respect to Cu and barrier characteristics should be high to ensure a sufficiently long TDDB (time dependency dielectric breakdown) lifetime, and the mechanical strength should be sufficient to withstand CMP (chemical-mechanical polish). At present, CVD and coating films each have advantages and disadvantages, and combining them will probably be necessary.

REDUCING PROCESS VARIATION

Robust Design of Circuits and Devices

As described in the previous section, the drive current heavily depends on the gate length and the gate insulation-film thickness. Variation resulting from this dependency must be reduced. Currently, manufacturing variation for each elemental process is analyzed in circuit simulations and device models at the circuit/device design stage, and the performance can be estimated, as shown in Fig. 4. This enables making early improvements to circuits and devices and enhancing their robustness.

In line with the above approach, Fig. 5 shows an example of calculating the sensitivity of variation in the drive current with respect to variation in each elemental process. In this example, the actual amount of variation generated in the manufacturing process for the gate length and gate insulation-film thickness as well as for the gate-electrode taper angle, various ion-implantation doses and energies, and temperatures of several thermal processes were used for the calculations. The results show that the drive current varies greatly with respect to the variation in gate length, gate insulation-film thickness, and gate-electrode taper angle and that it is relatively insensitive to variation in other processes. Furthermore, the reason the drive current is highly sensitive to variation in the gate-electrode taper angle is that ion implantation is done by highly accurately controlling the angle using the gate electrode as a mask.

To deal with such highly sensitive parameters, we need to determine how to improve the robustness of circuits and devices in design as well as how to reduce the manufacturing variation itself. Although a target value is also given for reducing variation in the ITRS, the difference between that value and the actual manufacturing variation is large, and a significant improvement of accuracy in manufacturing is therefore needed.

Advanced Process Control Technology for Reducing Variation

APC is expected to be a technology that can significantly reduce variation in manufacturing technology. Fig. 6 shows an example of applying APC to reduce variation in the gate length. In this system, a

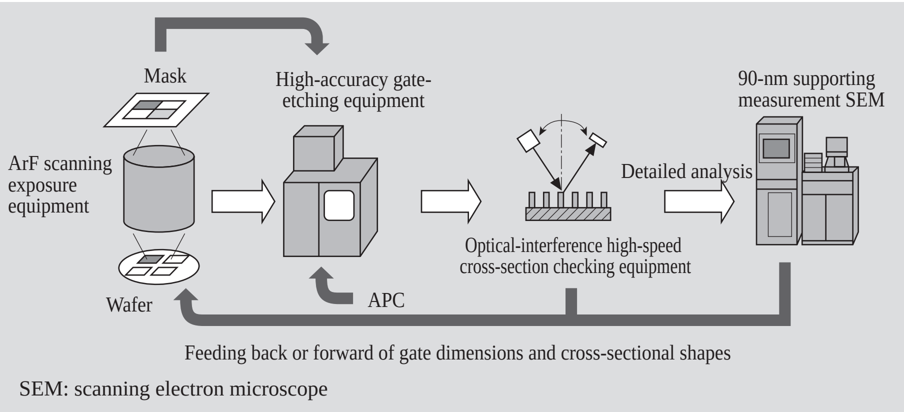


Fig. 6 —APC for Reducing Variation in Gate Length and Gate Shape.
Optical-interference-type high-speed dimension/cross-section measurement technology is incorporated in lithography and dry-etching equipment and the obtained data is fed back or forward for precise control.

high-speed dimension/cross-section measurement technology using an optical-interference system is incorporated in the lithography and dry-etching equipment and the obtained data is fed back or forward for precise control. Systems of this kind that can combine improving uniformity in each elemental process within a wafer with preventing changes in these processes over time need to be developed urgently.

CONCLUSIONS

Given that a CMOS platform can be standardized, determining how to achieve a production technology capable of high-yield manufacturing and short TAT (turnaround time) is important. In this regard, all processes and equipment involved in manufacturing must be systematically connected by applying technologies such as advanced process control and manufacturing variation must be reduced to improve the LSI frequency-allotment ratio and the chip yield.

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