High-current Ion Implanter for 300-mm SIMOX Wafer Production

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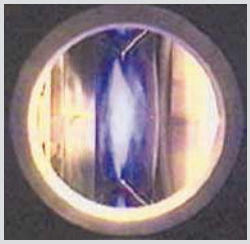
OVERVIEW: There is an increased demand for the production of next-generation super-high-speed and low-power-consumption CMOS (complementary metal-oxide semiconductor) devices using SOI (silicon on insulator). Major global device manufacturers are actively commercializing this product. In SOI technology, a device is fabricated in a silicon layer (SOI layer) formed on a BOX (buried oxide) film. Along with such high integration, the technology to support the creation of ultra-thin SOI layers of just 30 to 100 nm is in great demand. SIMOX (separation by implanted oxygen) is a technology that enables the creation of a BOX layer and SOI layer by implanting oxygen ions in a silicon substrate. Through the precise control of the ion beam, this method has a significant advantage in that the depth, thickness, and uniformity of the SOI and BOX layers can be freely controlled. Because such SOI substrates can be formed by simply implanting ions and performing thermal annealing after the implantation, the process can easily be simplified and made more cost effective. Hitachi High-Technologies Corporation has just commercialized its new ion implanter for 300-mm wafers, which is based on its last oxygen ion implanter for 200-mm SIMOX wafers. By introducing a high current (80 mA to 100 mA) to obtain high throughput, uniform implantation using the mechanical scan method, high-quality implantation through absolute cleanliness, and fully automated operation to accommodate production line needs, stable device operation is implemented to produce the highly uniform SOI films required for the next-generation SOI substrates. This device can be considered the driving force behind full-scale mass production of 300-mm SIMOX wafers.

INTRODUCTION

THE rapid development of IT (information technology) has invoked the need for high-speed, power-saving specifications in the fields of network information processing units and multifunctional portable terminals. The primary element of the above equipment, the CMOS-LSI (large-scale integration), has been better integrated by fine processing to enable the high-speed processing of vast quantities of data. However, processing speed is reaching its limit due to the thermal density caused by such fine structures. As evidenced by the adoption of SOI substrates and the development of new materials for use in copper wiring and Low-K materials, a breakthrough in high-speed processing is being promoted.

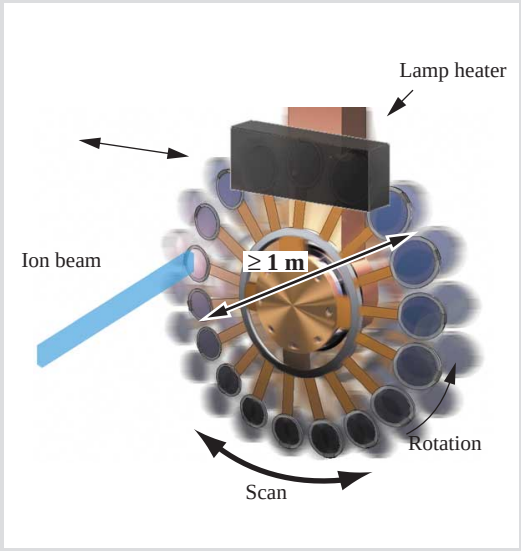
Recently, the world's major chip manufacturers have begun using SIMOX wafers, a SOI substrate, and actively developing high-speed devices of the THz class featuring super-low power consumption, which is more than a factor of ten smaller than the power consumption of conventional types. When these devices are mass-produced in several years time, the application of 300-mm SOI wafers is expected and those with 50- to 100-nm or thinner SOI layers will be required to realize high-speed processing.

In 1995, Hitachi released its ion implanter to produce 200-mm SIMOX wafers[1)]. Based on the wafer-production technology that evolved in the development of the ion implanter, Hitachi High-Technologies Corporation started marketing a new version oxygen implanter for 300-mm wafers in January 2001 in response to customer demand. This paper describes the characteristics and configuration of Hitachi's new ion implanter, the quality of the SIMOX wafers produced, and the vision for the future (see Fig. 1).



(a) 100 mA O^+ beam shape at implant chamber

(b) Microwave ion source



(c) SIMOX oxygen ion implanter chamber

Fig. 1—Characteristic Components of Hitachi's New High-current Oxygen Ion Implanter for Mass Production of 300-mm SIMOX Wafers.
The combination of experience in high-quality SIMOX wafer production technology accumulated in the high-current ion implanter for SIMOX and Hitachi's technology in the generation and control of high current ion beams has enabled implantation which produces ultra-thin, high-quality SIMOX wafers 300 mm in diameter.

NEED FOR SOI WAFERS

Through the research and development ongoing in various fields, the methods recently used to produce SOI substrates have been focused on SIMOX and bonding techniques.

Fabricating a CMOS-LSI, the leading edge in semiconductor device technology, on SOI substrates instead of conventional silicon substrates, will result in device performance ahead by one to one and a half generations. This is why major device manufacturers around the world have been actively engaged in the development of SOI devices.

The 2001 version ITRS (International Technology Roadmap for Semiconductors) roadmap forecasts that SOI substrates will increase from 200 mm to 300 mm in diameter and the SOI layer on which such devices are formed will become as thin as 50 nm to 100 nm or thinner for a device with 0.09-μm nodes. To unify the device characteristics, the surface uniformity of the SOI layer must be ± 2.5 nm (± 5%) or less. It is no exaggeration to say that the development of SOI technology depends on the stable, mass production of thinner and uniform SOI substrates like this. SIMOX enables the simplified production of thinner and more uniform SOI layers and BOX films by carefully controlling the ion beam energy. The development of high-current oxygen implanters for mass-produced 300-mm wafers is in great demand.

CONFIGURATION

Design Concept

When developing the new ion implanter, the basic beam-line configuration used was the same as that of the last version for 200-mm wafers. Additionally, techniques have been improved to attain a higher throughput, uniform implantation, and cleanliness. Fully automatic implant operation has also been incorporated. The typical development technologies are as listed below:

(1) High-current beam extraction from the oxygen microwave ion source
(2) Improvement of beam transport efficiency resulting in the increased implant current
(3) Adoption of the mechanical scan method and improvement in its controllability.
(4) Reduction of heavy metal and particle contaminations
(5) Fully automated operation using a PC (personal computer) screen and visual control of the operation progress

Table 1 shows the specifications of the Hitachi's new ion implanter.

Configuration

Fig. 2 shows the configuration of the Hitachi's new ion implanter [2]. This implanter consists of microwave ion sources that generate high-current oxygen beams,

a mass separator to select atomic oxygen ions (O^+) from beams extracted from the ion source, a post-acceleration tube to accelerate the energy to the desired level by additionally accelerating the ions, magnetic Q (quadrupole) lens to control the beam's cross-sectional shape, a 30° deflecting magnet to eliminate neutral oxygen atoms contained in the ion beams, and an implant chamber for the 300-mm wafers. The basic beam-line system is the same as that used in the last version. However, each component has been individually upgraded to cope with the demands of a higher current and mass production. For example, in terms of the ion source, a current increase through the optimization of the extraction electrode configuration and an upgrading of the vacuum level in the beam extraction area have been implemented to realize over 1,000 hours of maintenance-free operation of the ion source. While the last version uses a two-stage acceleration tube, the new one uses a multi-stage acceleration tube to enable stable voltage application. The Q lens to control the beam shape has been changed from the magnetic triplet system (used in the last version) to a doublet system to ensure a compact structure.

The batch implant system is used to implant a number of wafers simultaneously. Wafers are mounted on a rotating disc. Uniform implantation is done by a pendulum-like scanning of the disc in the radial direction. Wafers to be treated can be heated to 500 to 650°C using a combination of a lamp heater and beam radiation power. Corresponding to the variation of the beam power, the heater power is varied to control so that the wafer temperature is maintained at a certain level. Temperature is kept below ±10°C so that the quality of SIMOX is not adversely affected.

If any foreign material contaminates the wafer surface during implantation, it forms a shadow under which a buried oxygen film will not be formed. This is called a pinhole defect, which causes deterioration in the device's characteristics. Therefore, reduction of such pinhole defects is one of the most important issues to be addressed for SIMOX wafers. The particulate contamination totally depends on how wafers have been mechanically held and particle transportation from the beam line. Hitachi's new ion implanter implantation chamber features a well-designed structure to protect against heavy-metal contamination and optimized material selection and implantation

TABLE 1. Specifications
The specifications have been determined based on user need and the last version ion implanter's performance.

Item	Specification
Implant energy	40 keV to 240 keV
Maximum implant current	100 mA (180 to 210 keV)
Wafer temperature	500 to 650°C
Implant angle	10° to 14°
Implant non-uniformity	< ± 1.3% (maximum/minimum within surface)
Heavy metal contamination	10^{10}/cm^2 level (Fe, Cu, Ni, Al, etc.)
Number of wafers to be implanted	12 (300-mm diameter), 18 (200-mm diameter)
Particle contamination	0.5/cm^2 (particle diameter > 0.2 μm)

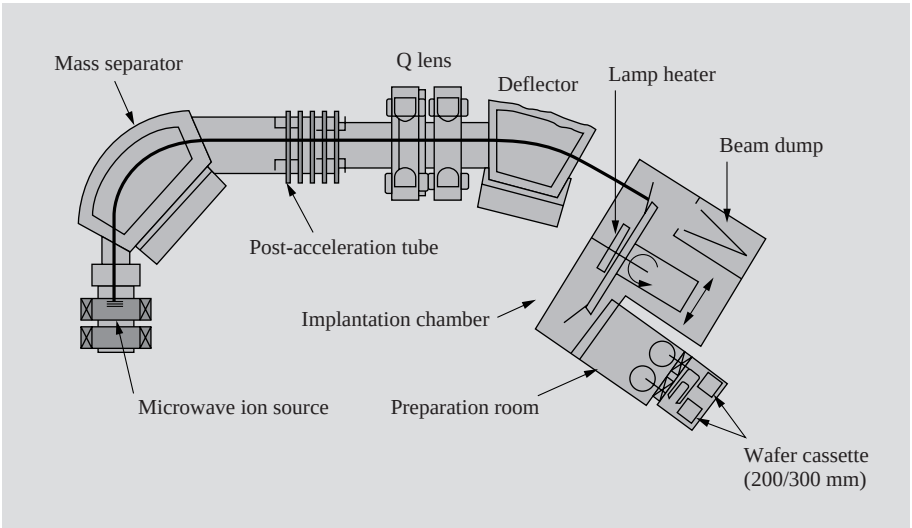


Fig. 2—Basic Configuration. Beam area on the wafer is about 40-mm wide and 100-mm high.

method, as well as for the reduction of dust.

IMPLANT PERFORMANCE

Implant Current

By adjusting the voltage of the post-acceleration tube, the new ion implanter allows implantation at various energy levels (see Fig. 3).

The figure shows that the new ion implanter enables the implantation of high-current oxygen ions over a wide range of energy. The shape of the ion beam on the wafer is adjusted to about 40 mm in width and 100 mm in height by controlling the magnetic Q lens at any energy level.

Implantation at 100 mA is stably performed in the energy range of 180 keV to 210 keV. The beam shape at 100 mA shown on the wafer well coincides with that obtained from the beam orbit simulation data from the ion source to the implantation chamber. The 100 mA ion beam shape has also proven to be fully controllable using the simulation results.

When implanting ions at $4 \times 10^{17}/cm^2$, the standard implantation rate for SIMOX wafers, at 100 mA, the new ion implanter requires about three hours for implantation. The implantation current variance is 10% or less while the average number of interruptions to implantation due to discharge of the ion source or post-level accelerating tube average is less than one. These facts assure great implantation stability.

To implant ions into wafers, the user need only to mount the wafer cassette and press the start button. The rest of the operation, including transportation of wafers, beam extraction, implantation, and ejection of implanted wafers, is performed automatically.

The ion source lifetime of more than a thousand hours is assured.

Reduction of Particulate Contamination

The most serious issue affecting SIMOX-SOI wafer quality is the reduction of pinhole defects in the BOX layer. A pinhole defect is ascribed to a particle (particulate diameter of 0.2 μm or more) adhered to the wafer to be implanted. Although sections shaded during implantation are often 'cured' through high-temperature thermal treatment of wafers in the atmosphere oxide, the most important is to reduce particulate contamination present during implantation in order to reduce pinhole defects.

We optimized the wafer holding method and holder material to reduce particle generation, and developed cleaning techniques to clean the beam line inner surface using diverged beams. As a result, particulate contamination of wafers transported from the beam line has been diminished. When checking a batch of wafers implanted with $4 \times 10^{17}/cm^2$ oxygen, a particle contamination level of $0.5/cm^2$ or less on the average has been obtained for particulate diameters greater than 0.2 μm. This value corresponds to a pinhole defect density of 0.1 to $0.2/cm^2$ or less after a thermal annealing treatment. This value satisfies the quality level required for an MPU (microprocessor unit) as shown in the ITRS 2001 version roadmap.

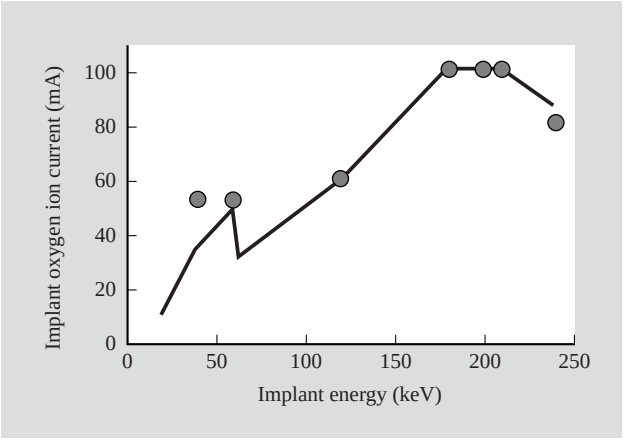


Fig. 3—Practical Implantation Current.
The solid line shows the values in the specifications. Black circles show practical implantation current values. Although results at 100 mA and 240 keV have been confirmed, only data obtained from prolonged implantation are presented in the figure.

SOI Layer Uniformity

For SOI devices, the SOI layer, on which a CMOS is formed, needs to be thinner and more uniform. Uniformity of the SOI and BOX layers totally depends on uniform implantation provided by the implanter. To evaluate the implantation performance of Hitachi's new ion implanter, we used an ellipsometer to measure the uniformity of the SOI layers of a 300-mm SIMOX wafer, which had been implanted and thermal-treated (see Fig. 4). The figure shows that a non-uniformity ±0.6% was obtained for the SOI layer. By adding the internal thermal oxidation process, which performs thermal treatment in a high-density oxygen atmosphere, SOI and BOX layers could be produced with a variance of ±1% (±1.5 nm) or less, thus, demonstrating favorable implantation characteristics.

The analysis of heavy metal contamination of the implanted wafers proved that the heavy metal contamination level for Cu and Fe, etc., was also

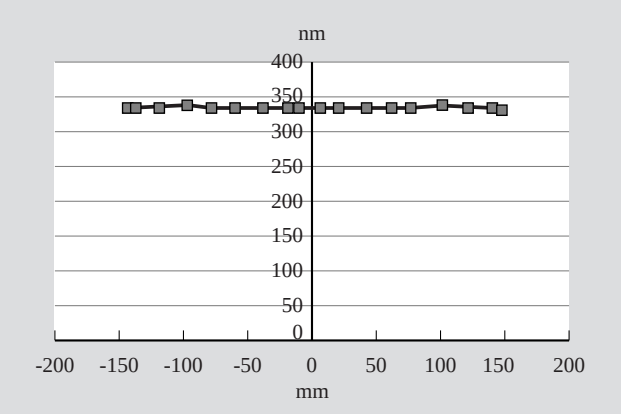


Fig. 4—SOI Uniformity for 300-mm SIMOX Wafers Produced Using Hitachi's New Ion Implanter.
The horizontal axis presents positions from the wafer center. The vertical axis presents the film thickness. Implantation is performed based on standard specifications at 180 keV/80 mA and $3.7\times10^{17}/cm^2$, and then thermal-treated at high temperature.

suppressed to a level of $10^{10}/cm^2$, assuring clean implantation for the new ion implanter.

CONCLUSIONS

This paper described Hitachi's new high-current oxygen ion implanter for 300-mm SIMOX wafers. This is the first implanter that enables the implantation of 300-mm SIMOX wafers using 100-mA high-current oxygen ion beams. The basic performance (film uniformity, particulate contamination, and heavy metal contamination levels, etc.) of the implanted SIMOX wafers fully satisfies the required specifications for the next-generation SOIs.

In the future, we will try continuous operation, etc., for implanter's applicability to mass-production lines, and check for operational reliability and determine if any improvements are warranted.

An attempt to form SIMOX on part of a wafer and mounting a SOI device and a bulk silicon device on the same wafer has been reported as well as the development of faster devices by mounting SiGe on SOI substrates. Practical use of SOI is about to take off.[3] We hope that Hitachi's new ion implanter will help to put high-quality, low-cost SOI wafers on the market and contribute to a major innovation in semiconductor technology.

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