Research & Development

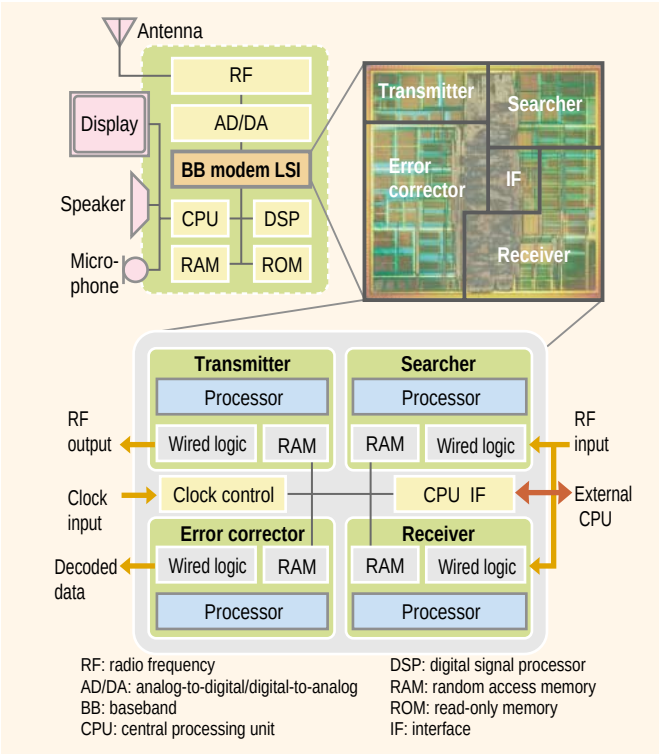
R&D is the key to enhance the industrial power and keep the stable social development. Hitachi is applying full effort in tackling the challenge of research and development for revolutionary advancement of the key technologies for the 21st century, including nanotechnology, the life sciences, energy conservation technology, and social-information infrastructure.

Baseband Modem LSI for W-CDMA Mobile Phone

A baseband modem LSI for W-CDMA (Wideband Code Division Multiple Access), a major standard of 3rd generation mobile communication systems, has been developed. This single chip was fabricated in a 0.25-µm CMOS technology to process digital signal modulation and demodulation for high-speed wireless data communication rates up to 384 kbit/s.

The LSI uses a newly adopted architecture called multi-engine, in which four software-controlled engines process the different functions required for data modulation and demodulation. Distributed processing by multiple engines enables a 1/6 lower operating frequency compared to the frequency required for a single processor architecture. Thus, the power dissipation of the LSI is lowered to 160 mW (with supply voltage 1.8 volts for the core, 3.0 volts for the I/O pins) during high-speed data communication. Furthermore, the programmability of the software-controlled engines enables extended flexibility in LSI design and shorter development periods.

The technology achieved through the baseband modem LSI development, together with technologies for other wireless components such as the RF-IC and RF-modules, will be further applied to provide the most advanced solution for W-CDMA mobile phone chip-sets.



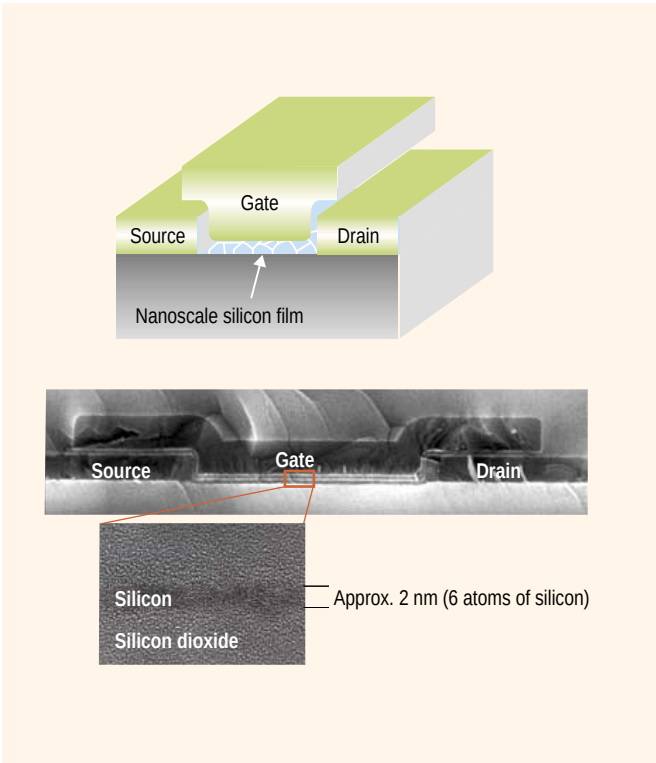
Structure of W-CDMA mobile phone terminal and the developed baseband modem LSI
The baseband modem LSI modulates and demodulates the CDMA signals.
(In the photograph of the chip, the rectangular area near the center is filled with logic gates, while RAM blocks are placed around the gates.)

Nanoscale Structure Memory for Mobile Electronics

A semiconductor memory device with the same capacity as a DRAM (dynamic random access memory) but operating at a 100 times lower power consumption has been developed. The experimental device shows remarkable promise as a low-power, large-capacity solution for mobile device memory application.

The demand for new applications in mobile electronic devices has made the use of large-capacity and low-power memory a necessity. Although the current DRAM technologies exhibit large capacity, the relatively high power consumption due to the leakage current of the DRAM transistors has prohibited the integration of DRAMs to mobile device LSIs.

A newly developed transistor resolves this issue. The transistor uses nanoscale silicon films having a thickness of the order of six atoms. Due to the small dimensions of the transistor, a quantum effect is induced that limits the leakage current to approximately a thousand times less than a conventional transistor, corresponding to a leakage rate of roughly one electron per second. A memory device based on this transistor has also been developed. The fabricated device achieved ultra-low power consumption due to the low leakage current of the transistor. The memory device is a promising candidate for the next-generation memories enabling users to enjoy multimedia applications without decreasing the battery life of mobile devices.



The schematic structure and the electron micrograph of the ultra-low leakage transistor

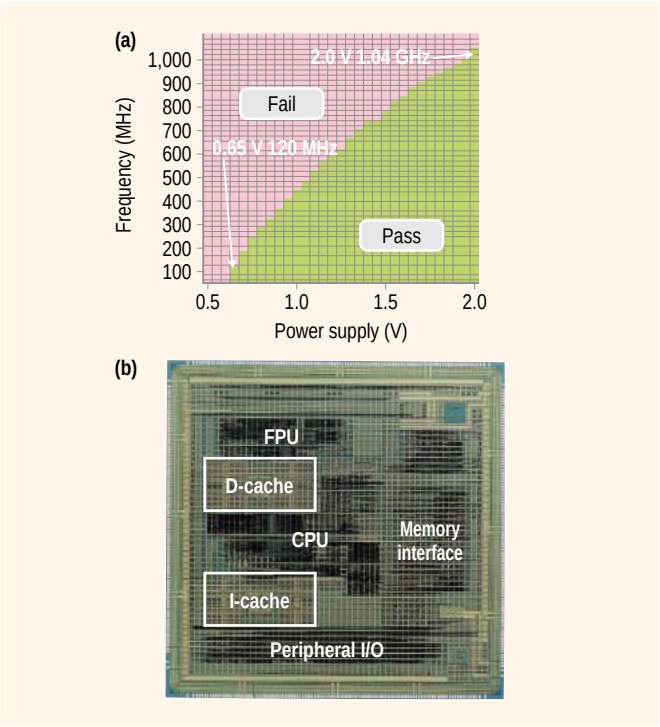
0.65-2.0 V Cache for Low-power-dissipation Microprocessors

An on-chip cache memory, which operates from as low as 0.65 V to 2.0 V, was developed for low-power-dissipation microprocessors. Such microprocessors are used for hand-held devices, such as third-generation cellular phones and personal digital assistants (PDAs), whose power consumption is reduced by varying the microprocessor-operation frequency and power-supply voltage according to system loads.

The developed cache realizes lower-voltage-range operation for lower power consumption and wider-voltage operation for higher performance of the next generation microprocessors.

Two key techniques were developed. One is a voltage-adapted timing-generation scheme that uses plural dummy cells to attain such a wide voltage-range operation. The other is a lithographically symmetrical cell (LS-cell) to attain lower-voltage operation.

The cache was fabricated by using 0.18-µm enhanced CMOS technology. The cache chip can continuously operate from 0.65 V to 2.0 V; its operating frequency and power are from 120 MHz at 1.7 mW and 0.65 V to 1.04 GHz at 530 mW and 2.0 V. At 120 MHz, the measured power dissipation is reduced by 97% compared with conventional power dissipation.



(a) Shmoo plot of the cache and
(b) RISC-microprocessor chip using the developed cache

Mobile Multi-lingual Automatic Interpretation System "Mobilingual"

A multi-lingual automatic interpreter system "Mobilingual" for cellular phones that is based on speech recognition technology was developed. The automatic interpreter has been generating great expectation as technological dream of the future.

The system can translate Japanese sentences registered beforehand into 10 different languages through a cellular phone. This process is preformed on a server located at the processing center.

The features of this system are as follows:

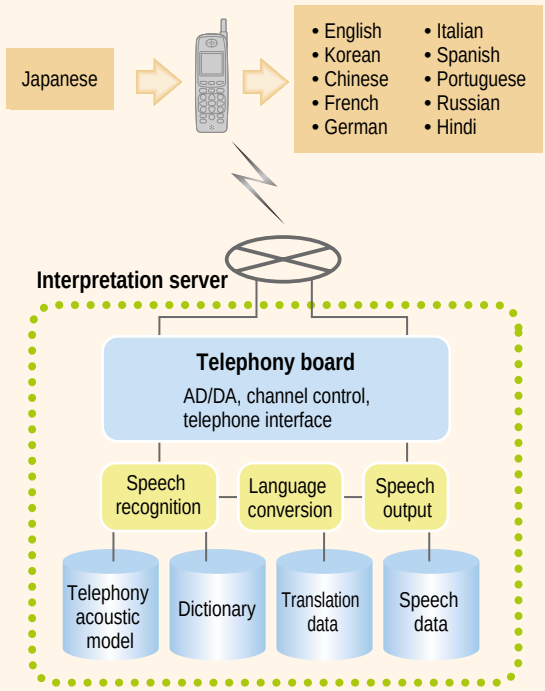
(1) The system can be used from any telephones.

(2) It is possible to recognize anyone's speech with high accuracy if they speaks clearly.

(3) The response is quick.

The opinions of potential users where sampled in a real-time experiment.

Our future work will focus on improving the performance of the system under adverse noise environments, and we will endeavour to develop the the concept of a new service that will ease social internationalization.



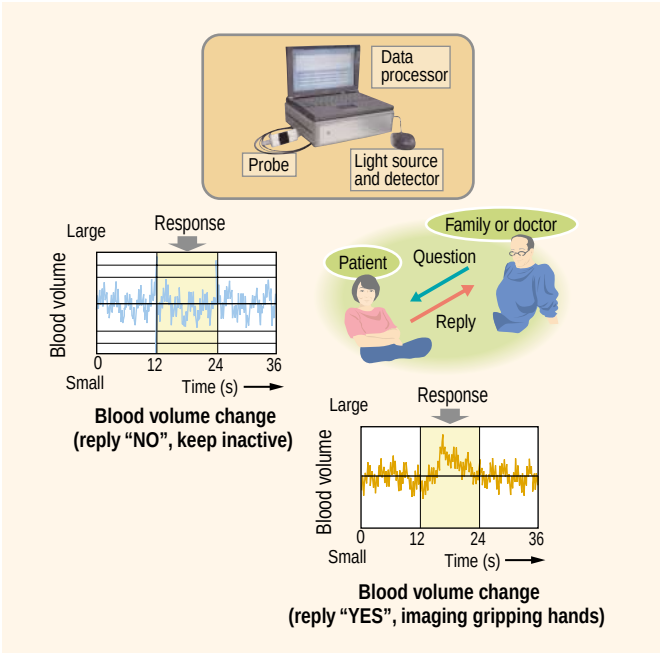
System and process
The Japanese speech uttered by a cellular phone user is recognized on the server at the center, and converted into 10 foreign languages.

ALS Patient's Communication Equipment

ALS (amyotrophic lateral sclerosis) is progressive obstinate disease that damages the motor nerves of the spinal cord. This results in the patient afflicted with ALS rendered unable to move their muscles at all so that they lose the ability to communicate. However, the ALS patient's brain functions work normally despite their body being wasted. We have developed a new communication tool for ALS patients that uses a brain function measurement method that utilizes near infrared light.

This communication tool works as follows: When the patient wants to answer yes to a question, we ask him to imagine gripping his hands, for example, then his brain function is activated, and blood volume in the cortex increases. When the answer is no, we ask him to stay still. Then the blood volume change is small. The new communication tool measures the blood volume changes in the cortex and informs us of a yes or no answer. The set up of the tool is as follows: A sensor connected to the light source and light detector is attached to the scalp of the patient, and the reflected light intensity changes are measured to estimate the blood volume changes in the cortex. Near-infrared light is employed to detect the change. The light penetrates the scalp and skull, and reaches the cortex to estimate the blood volume change in the cortex. The reflected light from the cortex is measured and analyzed by the data processor to estimate the blood volume changes at the cortex.

We expect to improve the practicability of this newly developed communication tool for ALS patients by downsizing the system and decreasing the measurement time. This research was performed in collaboration with the Department of Medicine, Tokai University.



Patient-communication equipment and change in blood volume
External view of the prototype equipment is shown. The two optical fibers shown next to the equipment are attached to the patient's head.

Position Sensorless Control Technique for High Efficiency Permanent Magnet Synchronous Motors

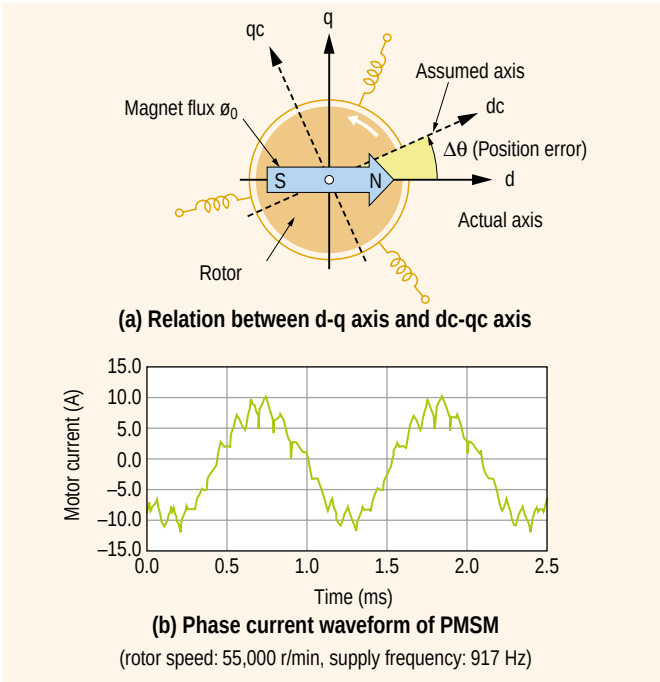
Permanent magnet synchronous motors (PMSMs) are widely used as actuators in many drive applications. PMSMs have several advantages, such as their small size, high efficiency and simple commutator-less construction, compared with conventional DC/AC motors. PMSMs are especially expected to provide the means for realizing energy saving drive systems in the near future.

Usually, a sensor that acts like an encoder to detect the rotor position of PMSM is required in order to drive PMSMs at arbitrary speeds. This sensor increases costs and reduces the reliability of PMSM drive systems. Therefore, if the sensor can be eliminated, a simplified structure with high reliability can be realized and the application fields are widened.

We developed a new control technique for PMSMs that does not need a position sensor. Eliminating this sensor was achieved by using "the direct position error estimation." The position error $\Delta\theta$, which expresses the error between the assumed rotor axis (dc-qc axis) and actual one (d-q axis), can be directly estimated by using our original equation. This equation is derived from the mathematical model of PMSM.

Based on the computed position error, the dc-qc axis is corrected, and the position error is controlled to zero. As a result, a high-performance PMSM drive system is realized. The control algorithm for this technique is so practical and uncomplicated, it can be implemented using a 16- or 32-bit microprocessor.

The results of an experimental evaluation demonstrated the superior characteristics of the PMSM drive system. This system proved that a PMSM can be stably driven up to 55,000 r/min. This technique has already been applied to air-conditioner compressors of industrial drive systems, etc. We are continuing our efforts to apply this technique to other products.



The principle of position sensorless control and the current waveform of PMSM

Next-generation Streaming Server System for Broadband Networks

The increasing availability of high-speed broadband Internet connectivity is driving the development of new multimedia applications such as video streaming. To ensure the success of services based on these emerging applications, high-performance and high-quality server systems are needed.

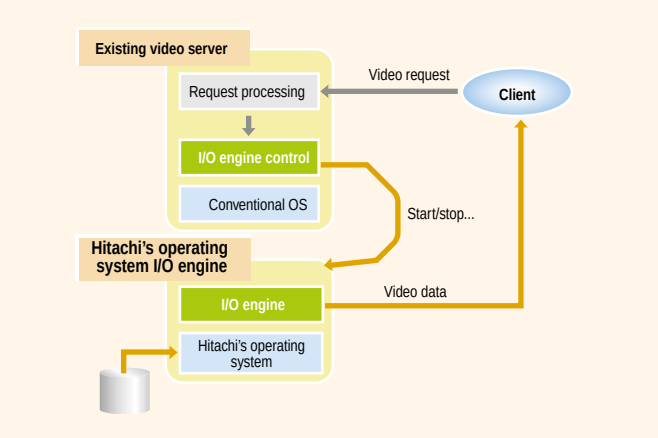
In response to this need, Hitachi developed a new real-time operating system that can deliver high I/O performance with quality of service (QoS) guarantees. It can be integrated within existing video server systems for performance enhancement using low-cost PC server machines (Intel* x86 processors).

The integration of the operating system within existing streaming systems is done using the external I/O engine architecture. This architecture is enabled by replacing the I/O processing part of video servers with an I/O engine control module, which drives the execution of the operating system external I/O engine. This approach minimizes the amount of modifications needed in existing video servers, thus keeping development costs low.

The external I/O engine architecture also preserves other services provided by existing systems, as well as the client / server interface for video request. Existing client software can be used without modifications. Tactix also ensures a virtual infinite scalability of system performance by allowing the use of several external I/O engines simultaneously.

A prototype system using an Apple QuickTime** Streaming Server (Darwin 4) integrating a single Tactix external I/O engine was developed to validate performance enhancements. The modified QuickTime server can deliver peak performance of more than 1,000 simultaneous video streams (QuickTime encoded MPEG1 stream at 1.5 Mbps) representing a data throughput of more than 1.5 Gbps. This represents a performance increase of more than 5 times the original QuickTime Darwin server, resulting in the best-ever cost-performance streaming server.

* Intel is a registered trademark or trademark of Intel Corporation in the U.S. and other countries.
** QuickTime is a registered trade mark of Apple Computer, Inc.



External I/O engine architecture can enhance stream server performance with low development cost
Our prototype system can deliver simultaneously 1.5 Gbps of stream data.

Fingerprint Verification System on MULTOS* Card for Secure Person Authentication over the Internet

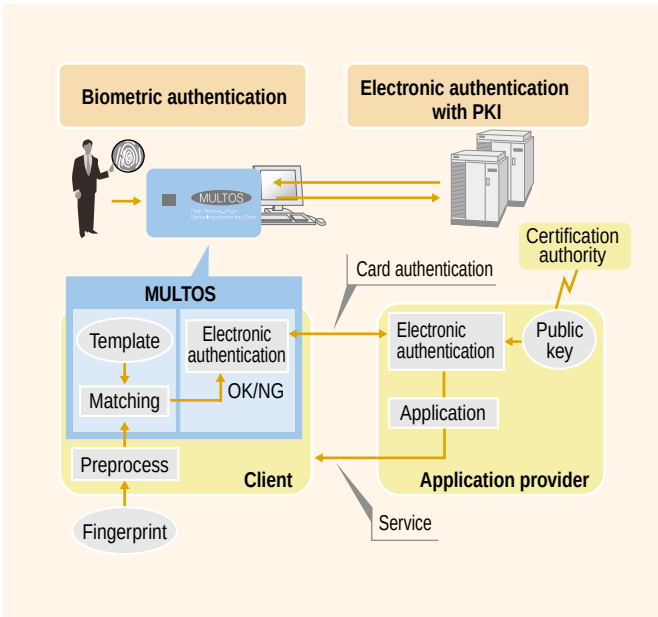
Secure person authentication is required for the safe conduct of electronic transactions over the Internet. In traditional person authentication with smart cards, the validity of the smart card and the user are confirmed based on the public key infrastructure (PKI) and passwords, respectively. Since using passwords could be a security hole, biometric authentication based on fingerprints has become the center of attention.

In applying fingerprint verification to Internet transactions, it is most important to prevent impersonation due to the alteration of fingerprint templates or the result of the verification. Executing the fingerprint-matching process using an unauthorized computer such as a client PC, could cause result in fraudulent use if template has been altered or the verification result is tampered with.

We developed a fingerprint verification system that operates on the MULTOS card, which is a kind of smart card having a tamper-resistant CPU and memory, in order to prevent fradulent use. In this system, the cardholder's fingerprint template and the fingerprint matching function are embedded in the MULTOS card. The smart card matches the template and the fingerprint image of the cardholder, then executes the electronic authentication process based on the PKI if the fingerprint matches the template. The function for electronic authentication is also embedded in the card.

Since the fingerprint template and the result of the matching are protected by the tamper-resistance of the card and cannot be revealed, highly secure person authentication is accomplished. This system was designed so as not to affect the general electronic authentication scheme in any way. Consequently, this system can be adapted to the existing electronic transaction systems that are based on the PKI.

*MULTOS is a registered trademark of mondex International Ltd.



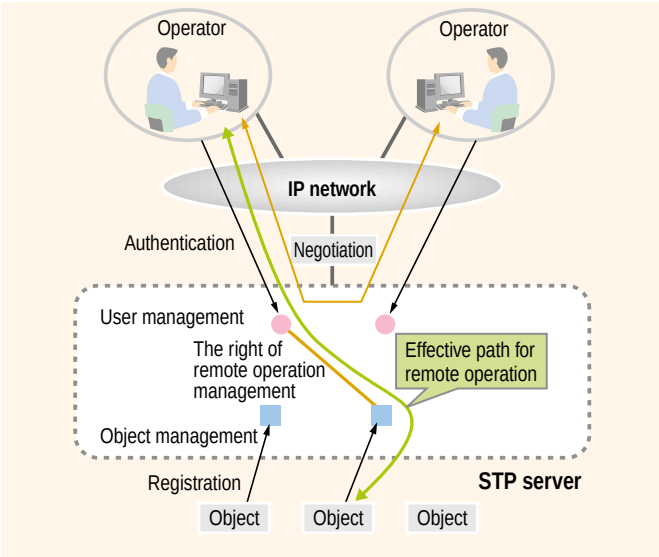
Configuration of fingerprint verification system embedded in the MULTOS card
Embedding the fingerprint matching function in the MULTOS card enables authentication of individuals with full linking between fingerprint verification and PKI.

Secure Tele-operation Protocol Supposing Several Authorized Operators Existing on IP Network

Recently, web-based monitoring systems have been introduced in many applications. It is presumed that such systems are helpful in various situations. The secure tele-operation protocol (STP) that we developed is an effective technology for controlling objects remotely on an Internet protocol (IP) network.

The most significant advantage of using a web-based system is that monitoring and controlling can be performed anytime, anywhere. This means that several authorized operators are able to exist on an IP network in different places and simultaneously. Moreover, many other people also exist on the same IP network, but who have no related functions. Our objective is to establish a remote operation technology that is fit for the age of the Internet. We must assure that the various operators will be able to carry out their roles without interference. However, what we have to eliminate is the potential for objects to be operated in an improper manner.

The main feature of the proposed system is its ability to use the STP server as an intermediary to safely manage remote operations. Now, it assumes that two authorized operators exist on an IP network as shown in the figure. In remote operation through an STP server, two operators cannot operate the same object simultaneously. In other words, a single operator who has the right of remote operation can function, however, the other operator is denied the right of remote operation. The right of remote operation is managed in the STP server. Furthermore, the right of remote operation can be safely transferred upon negotiation by the operators. We will introduce this technology for web-based real-time remote operation for application to many fields.



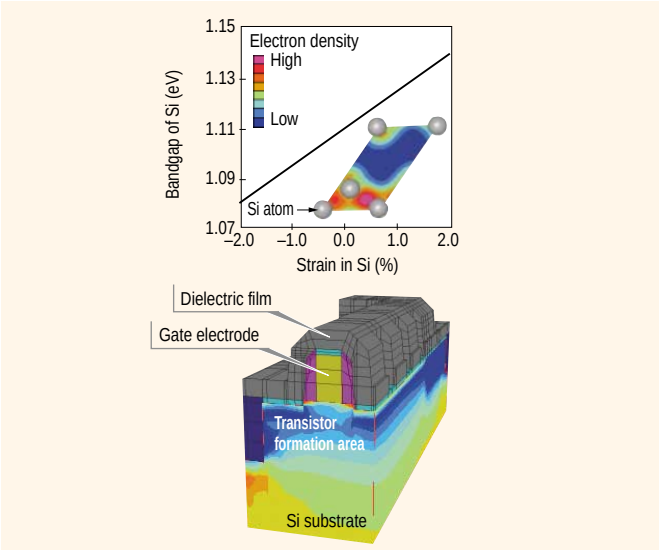
Outline of remote-operation technology incorporating the right of remote operation functionality
The STP server dynamically combines operators on the network and target objets. Rights can also be transferred between operators.

High-performance Si MOSFETs Using Mechanical Stress Control of Thin Films

High-speed transistors are the key component for large-capacity signal transmission and processing. Using strained silicon technology is an effective way to improve transistor performance. This improvement is based on the bandgap narrowing of Si by applying a SiGe layer, which has a lattice constant larger than that of Si, just under the transistor formation layer. Though such a biaxial tensile strain field is effective for the enhancement of the performance of n-MOSFETs (n-type metal-oxide-semiconductor field effect transistors), an anisotropic strain field is necessary to improve the performance of p-MOSFETs. This is because of the bandgap splitting of the donor level and the acceptor level of Si, and it is explained by the first principles calculation. An additional strain control method is, therefore, indispensable for producing high- performance CMOS (complementary MOS) circuits.

The internal stress of the thin film materials used in deep-submicron devices often exceeds 1 GPa. Such high stress causes a serious change in the strain field of transistor structures. For example, thermal oxidation of a Si substrate results in very high compressive stress in the substrate, and gate electrode materials, such as tungsten and silicon nitride, hold tensile stress higher than 1 GPa. Therefore, an anisotropic strain field can be controlled by applying these stress development mechanisms properly. The final strain field in transistor structures is predicted quantitatively by a three-dimensional finite element analysis considering not only thermal stress but also the intrinsic stress of thin films. The optimum transistor structure can be designed by using the results of this analysis. The optimum strain field for CMOS circuits is achieved by changing the layout pattern of the circuit (shape of isolation areas), material combination of gate electrodes, plane shape of dielectric thin films, and the intrinsic stress of all the thin films. The increase in operating frequency of the optimized transistors has sometimes exceeded 30%.

This anisotropic strain control of transistor structures enables us to produce high-performance transistors efficiently in a short time. We believe high-performance transistors will contribute to the comfort and convenience of daily life that is brought about by electronic devices.



Predicted change in bandgap of Si based on the first principles calculation (top) and analytical result of a three-dimensional strain field in a transistor structure

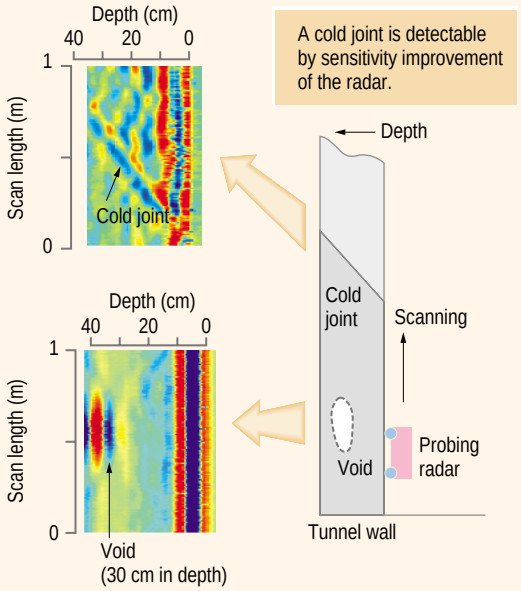
Microwave Radar for Probing Concrete Structures

Concrete structures, such as tunnels or buildings have attracted concern because of the fear of their concealing deterioration resulting from long time use under severe conditions. Non-destructive inspection methods to evaluate in-service structures, therefore, have been pursued vigorously.

Microwave radar is effective for inspecting the interior of concrete, but it is difficult to probe deterioration reliably from the shallow to the deeper regions because of a large amount of surface reflection and the high attenuation rate of wave propagation that occurs inside of a concrete structure.

Hitachi, Ltd. and Hitachi Engineering & Services Co., Ltd. developed a high-sensitivity probing radar. The radar uses electromagnetic waves 10^{-9} second wide, and displays internal flaws or voids as a reflection strength image in sections along the radar scanning line on the structure surface. The sensitivity of the transmitting and receiving antennas is improved effectively by numerical value analysis. Transmitting power is increased as the observed points become deeper. This sophisticated power control method reduces the level of surface reflection and improves detection sensitivity by overcoming the attenuation of wave propagation.

The radar has demonstrated sensitivity that is more than 10 times that of our earlier equipment, when used to probe experimentally several test sections of tunnel wall containing artificial voids. It also can detect a cold joint, which is a boundary created when two adjacent sections of concrete are poured at different times. These joints have been difficult to probe until now.



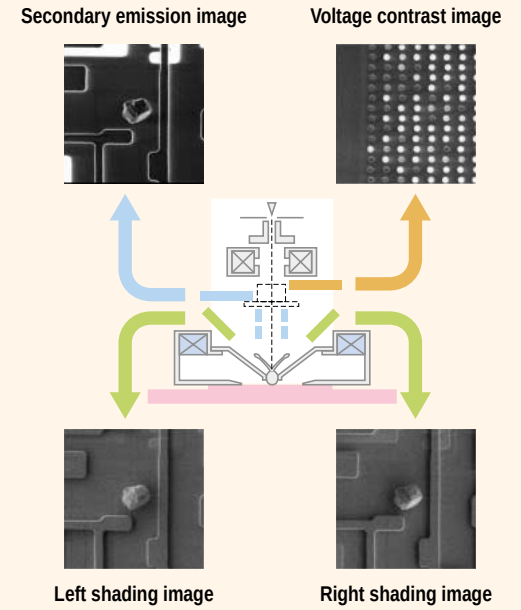
Examples of tunnel-wall inspection by radar
Displays of previously undetectable concrete cold joints and internal voids detected using probing radar with improved sensitivity.

Image Processing Algorithm for Automatically Classifying Defects Smaller Than 0.1 µm

Semiconductor refinement is making remarkable advances. Defects smaller than 0.1 µm are currently posing manufacturing problems, and there are many different types of defects. Defect detection and type identification is necessary in order to pinpoint abnormalities in the manufacturing process.

For the quantitative identification of a defect, automatic defect classification (ADC) was developed as an algorithm for classifying a defect photographed under a scanning electron microscope. This algorithm extracts contrast, shape, and other defect information from photos obtained by a special detector developed for defect observation and automatically classifies and identifies a defect based on the obtained information. The ADC capable of processing 600 defects per hour increases the efficiency of manufacturing remarkably compared to conventional visual observation.

This newly developed algorithm is incorporated in the scanning electron microscope, which has been designed specifically for defect observation.



Configuration of ADC-mounted review scan electron microscope
Multi-aspect defect information is acquired by multiple electro-optical systems for accurate defect identification.