Layout Design and Lithography Technology for Advanced Devices

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OVERVIEW: The minimum feature size required for the most advanced semiconductor devices is now below half the exposure wavelength, and the optical lithography technology is facing its practical resolution limit. In this article, we review the current status of DFM and issues for further miniaturization. The role and requirements of metrology technology are also discussed. The layout design has been implemented following the device design rules required for device characteristics and layout design rules required for lithography technology. On the other hand, lithography technology has pursued accurate replication of designed patterns on a wafer. However, as required minimum feature sizes decrease to 45 nm or smaller, severe deformation of replicated patterns occur due to optical proximity effects, and the process window becomes very narrow for mass production. As a result, researchers in layout design technology needs to consider not only circuit characteristics but also lithography characteristics, which are part of DFM.

INTRODUCTION

THE development of ULSI (ultra-large scale integration) devices has been led by the miniaturization of semiconductor devices and optical lithography technology played a major role. However, the optical lithography is now facing its practical resolution limit. To overcome the situation, we need to pursue its ultimate resolution limit(1). Circuit design has been

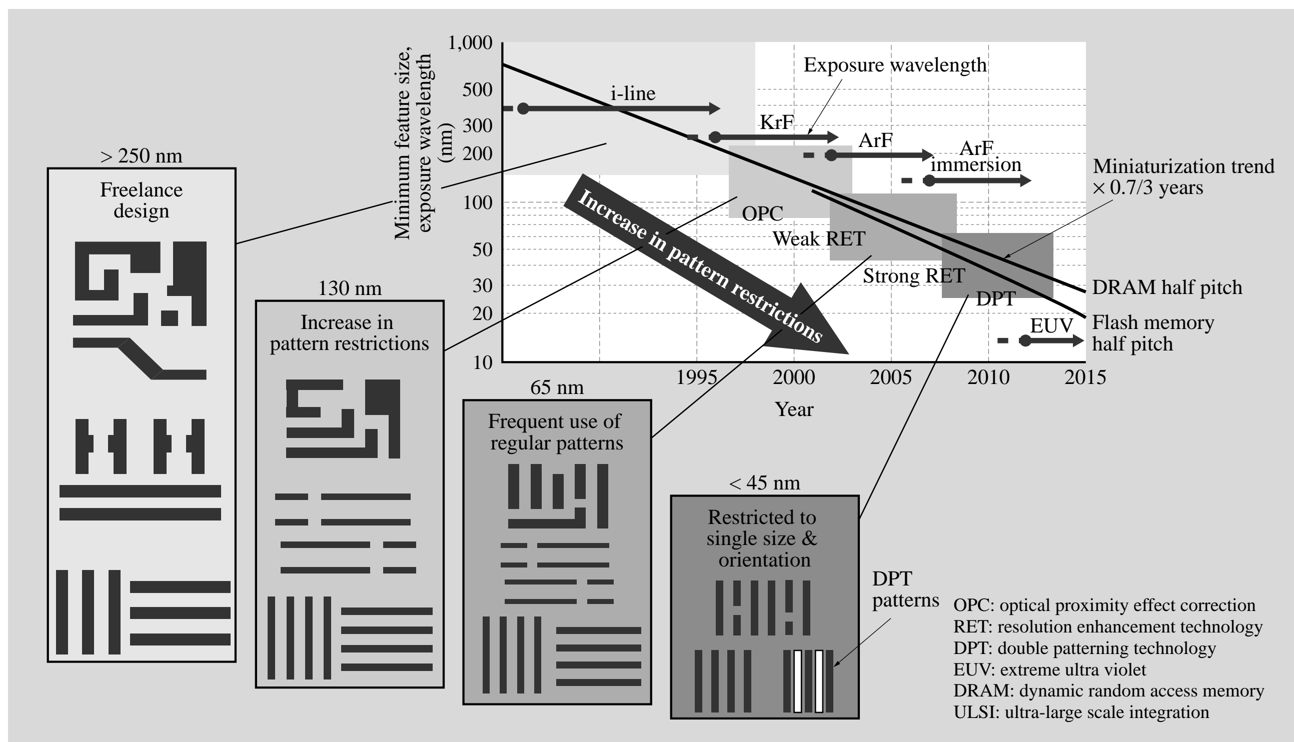

Fig. 1—Trends of Device Miniaturization and Layout Design Constraint.
Layout design for advanced devices requires consideration of lithography characteristics as well as circuit characteristics. This is a DFM (design for manufacturability) technology.

implemented following device parameters and design layout rules. In such a situation, there was no need for layout designers to take into account lithography technology in detail. On the other hand, lithographers have been pursuing accurate replication of designed patterns on a wafer. But device and layout designers are forced to take lithography characteristics into account as well as circuit characteristics recently (see Fig. 1). This is one of the so-called DFM (design for manufacturability) technologies.

Although EUV (extreme ultra violet) technology has been developed as the next-generation lithography, we have to extend current optical lithography at the moment because the fundamental difficulties related to EUV lithography still remain[2]. Furthermore new device structures and materials such as strained Si, high-*k*, and metal gate technologies, are also required for improving the device performance as well as device miniaturization.

First, issues of optical lithography are reviewed. Next, the design strategy to overcome those issues will be discussed. The current status and issues of DFM will be then reviewed, and finally the role and requirements of metrology technology will be discussed.

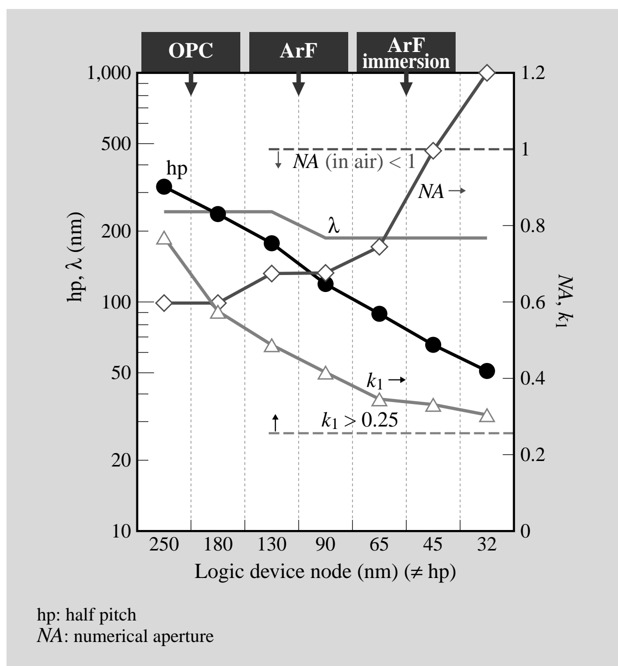

Fig. 2—Trends of Exposure Wavelength λ, NA, and k_1 Factor.
Miniaturization was attained by optimizing λ, NA and k_1 with diversifying risks. The k_1 factor for the most advanced devices is below 0.4. Logic device node proceeds one generation compared to DRAM half pitch node.

DFM FOR DESIGN OF ADVANCED DEVICES

Issues in Optical Lithography for Further Miniaturization — Low-k_1 Lithography —

We describe the resolution of optical projection lithography using the following Rayleigh's formula[3];

$R = k_1 \times \lambda / NA$,

where λ is the exposure wavelength, *NA* is the numerical aperture of projection optics, and k_1 is a constant depending on the lithography process. As k_1 decreases, the lithography becomes more difficult. The theoretical lower limit of k_1 is 0.25 for the projection lithography system with the interference of two or more plane waves.

We have addressed technical challenges for the new technology generation in terms of λ, *NA*, and k_1, and developed all together in the past. We were able to effectively develop lithography technologies, and diversify development risks. The typical values of λ, *NA*, and k_1 from recent papers are plotted in Fig. 2. The horizontal axis in Fig. 2 is the logic device technology node, which proceeds by one generation compared to DRAM (dynamic random access memory) half-pitch node.

The current exposure wavelength used in the most advanced optical lithography is a 193-nm ArF excimer laser. An F_2 laser with shorter wavelength of 157 nm was investigated as a successor of the ArF in the past, but it was abandoned due to the difficulties in developing optical materials and relatively small resolution gain[4]. EUV lithography with a wavelength of 13.5 nm, which is shorter than a tenth the wavelength of the ArF laser, is now under development as the next-generation lithography technology[5]. However, still many critical issues are remaining and it may take several years to solve them.

The theoretical limit of *NA* was 1 for the conventional lithography system. But recent development in immersion lithography technology has enabled *NA* to be higher than 1[6]. Water is inserted between the last lens of the optics and a wafer in immersion lithography, which increase *NA* up to 1.35. We can increase *NA* more by using higher index materials, but there are still many issues remaining related to materials for practical application[5].

The k_1 factor is now going below 0.4, and we have to pursue an even lower k_1 further since there is no prospect for improvement of λ and *NA* at the moment. The k_1 is a kind of index which represents the pattern fidelity on a wafer to mask patterns, the extent of the process windows, and sensitivity to process variation. The relation between k_1 and pattern fidelity is shown

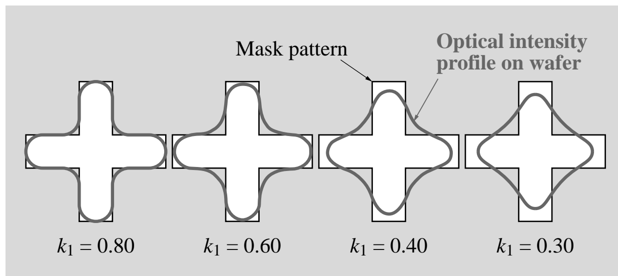

Fig. 3—Degradation of Pattern Fidelity Due to Lowering of k_1.
Severe pattern deformation was observed at $k_1 < 0.4$.

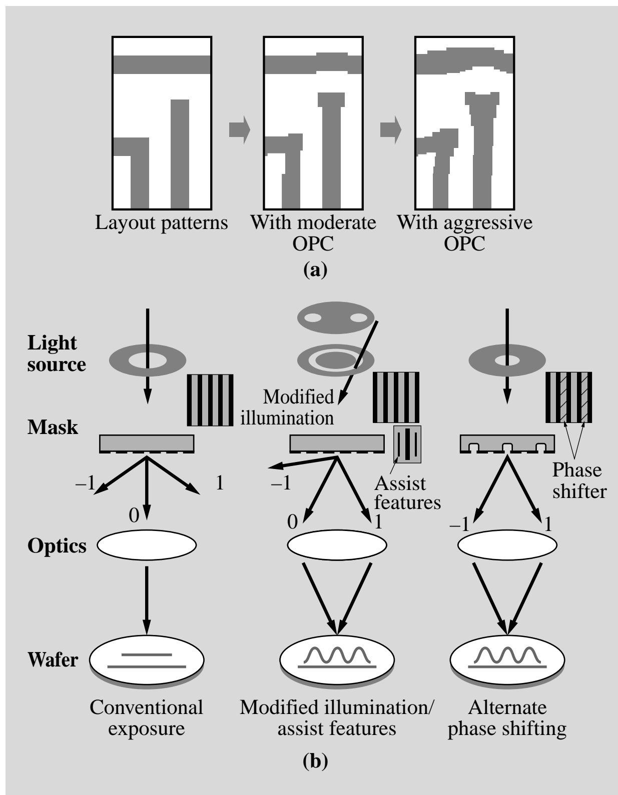

Fig. 4—OPC and RET.
Examples of OPC (a) and various kinds of RET (b) are shown.

in Fig. 3. We can see rapid degradation of the pattern fidelity of k_1 of around 0.4.

The pattern fidelity becomes particularly degraded in k_1 region below 0.35, and this region is called low-k_1 lithography. The following are problems of low-k_1 lithography; (1) degradation of pattern fidelity, (2) narrow process windows, and (3) high sensitivity to process variation such as mask manufacturing errors and optical element errors of exposure tools.

Under such situations, we are forced to pursue the limit of the following two technologies to overcome these problems as described in Fig. 4.

(1) OPC (optical proximity effect correction)[7]; the technology that corrects mask pattern shapes so that the projected pattern shapes are as close to the layout pattern shapes as possible. Examples are shown in Fig. 4 (a).

(2) RET (resolution enhancement technology)[8]; the technology that improves the resolution and enlarges the process windows. Phase shifting, modified illumination, and assist features techniques are examples of RET shown in Fig. 4 (b). Strict constraints on pattern shapes and arrangements are required to improved resolution to a large extent.

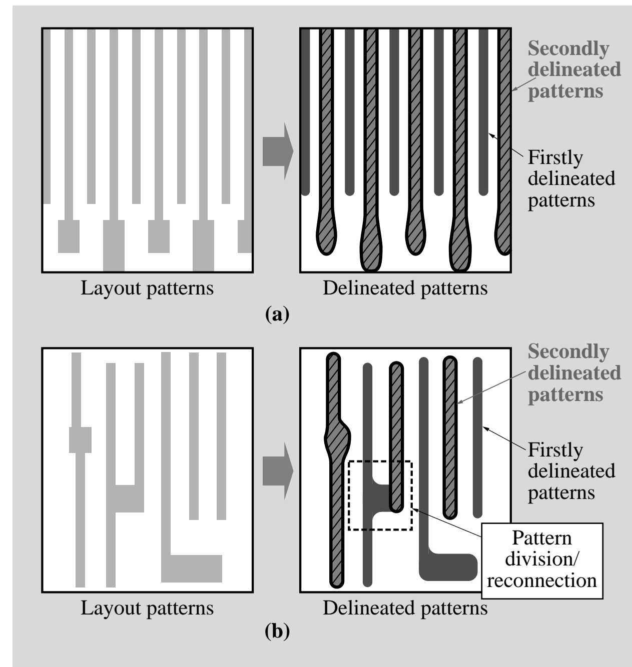

Fig. 5—Examples of Double Patterning.
Memory applications (a) and logic applications (b) are shown.
In double patterning, two relaxed patterns are superimposed.
Pattern splitting, reconnection overlay accuracy, and process costs are the issues.

A technology that reduces k_1 factor is proposed as a double patterning technology[9]. The fine pitch patterns are split into two, and delineated separately as shown in Fig. 5. There are possibilities of reducing k_1 below 0.25, but issues of pattern splitting, pattern reconnection, tight overlay control, and increase of process cost must be overcome before practical use.

Issues in Low-k_1 Lithography

More regulations on pattern design are required in low-k_1 lithography to make RET more effective. Pattern constraints have been integrated in design layout rules, and designers have been designing circuits according to them. As the pattern size decreases, the

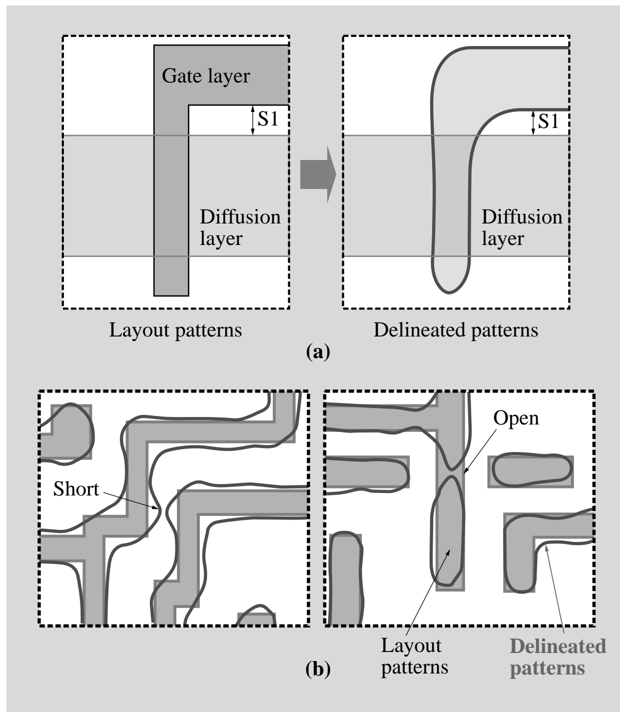

Fig. 6—Examples of Systematic Defects.
Pattern deformation in two-dimension causes systematic defects (a). Narrow spacing, S1, is the issue. Shorts and openings occur due to narrow process window (b).

more constraints on a pattern design are needed. A report shows that the number of layout rules has tripled in a 45-nm node from 180 nm(10). We believe the reason is that RET imposes more pattern regulations, requires a more complicated OPC, and that a relatively larger ambit affects pattern formation.

The two-dimensional deformation of patterns increases in low-k_1 lithography, and we cannot avoid the rather large discrepancy between the delineated patterns and layout patterns, as shown in Fig. 6 (a), where a corner part of a gate pattern exists, even though a complicated OPC is applied. If this corner is located near the active area, it may affect device performance(11). We need to place such a part well apart from the active area, or make a simpler and straight design layout.

We need to verify the manufacturability whether we have enough process window for manufacturing on the actual design layout due to the narrowness of these windows in low-k_1 lithography(12). Process window aware design is required along with stringent process control in manufacturing. Exposure dose and focus position are considered as major variations in lithography, and mask manufacturing errors are also becoming a major factors. Fig. 6 (b) shows an example of the lack of process windows in actual layout patterns.

Specific patterns with unacceptable pattern deformation or a lack of process windows described above are called systematic defects or hotspots. One systematic defect reduces manufacturing yield significantly, unlike a conventional random defect.

Detection of Systematic Defects and Solution through DFM

It is difficult to remove systematic defects by design rules in advance because the combination of a complicated actual layout and the type of RET causes systematic defects. The detection of systematic defects through simulation has been intensively investigated. We can now detect them with a certain accuracy because of development of accurate models based on optical

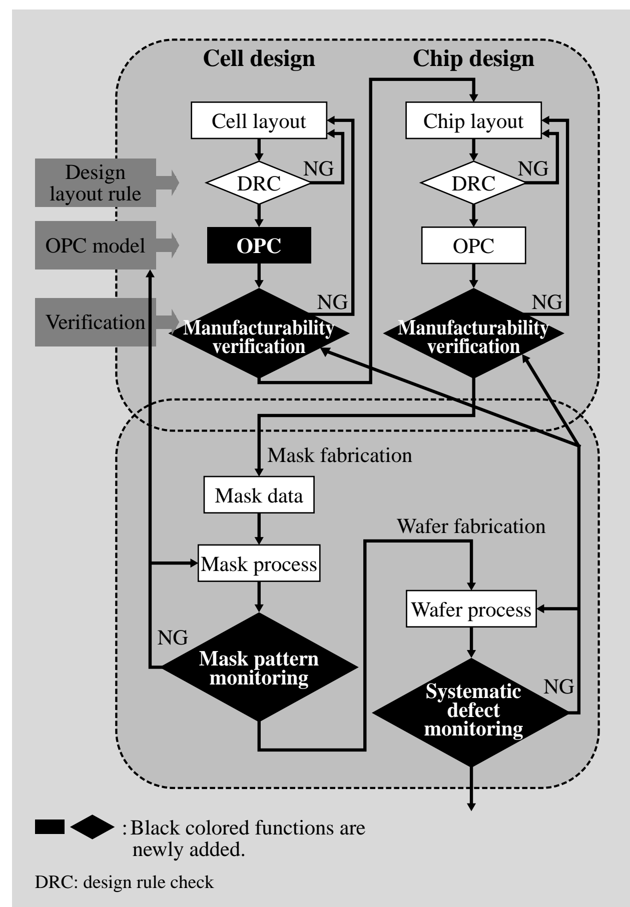

Fig. 7—Manufacturability Aware Device Design Flow.
To remove systematic defects, manufacturability verification is performed at cell and chip design levels. If systematic defects are found at the verification stage, layout correction and manufacturability and circuits verification will be repeated until all the systematic defects are removed. Black colored functions are newly added.

simulation and high-speed computing technology. This is called computational lithography, which is active utilization of simulation for the prediction of pattern shapes and process optimization. It is becoming more and more important to improve simulation accuracy for pursuing low-k_1 lithography and integrating lithography technology into design technology.

Fig. 7 shows an example of device design flow taking manufacturability into account(13). A simulation is used for verification of manufacturability for all the design patterns in a chip in addition to the conventional DRC (design rule check). If a systematic defect is detected, modification of layout and verification of circuit characteristics and manufacturability are iterated so that all the systematic defects are removed. Design and lithography technologies can no longer be considered separately.

We often encounter situations in which we can easily modify layout in the early stage of design, but it becomes difficult in the final stage. Verification of manufacturability for layout patterns should be leveraged from the early stage of cell design.

THE CURRENT STATUS AND FUTURE PROSPECTS OF DFM

The Current Status of Design Tools for DFM

Design tools, such as EDA (electronic design automation) are key factors for achieving DFM on actual devices designs. Design tools are required to connect between design and lithography, and new functions, such as OPC, verification of manufacturability, and automatic modification of systematic defects are needed in addition to existing functions of DRC and mask data preparation.

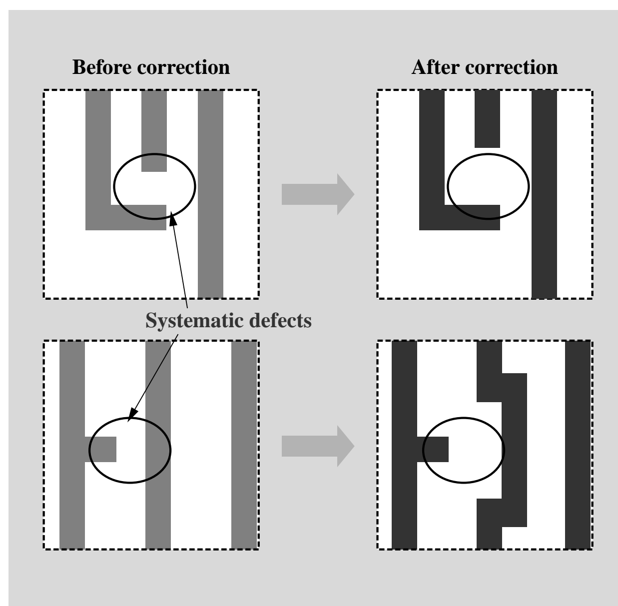

Fig. 8—Defect Repair Using EDA Tool.
Systematic defects can be automatically repaired with EDA (electronic design automation) tools.

To realize these new functions, the following capabilities are required; (1) handling of large-scale data for chip level design, (2) an accurate simulation model and calculation, and (3) fast processing time. These new functions have been developed by EDA vendors and device manufacturers. The development is also accelerated through new EDA vendors focusing mainly on new functions and collaborating with device manufacturers.

Fig. 8 shows examples of modification of systematic defects in which current design tools are applicable. We can reduce designers' tasks by modifying design layout automatically or indicating candidate modifications. There was a report that 94% of 2,500 systematic defects were modified automatically in 100 minutes for the gate layer of a 65-nm node ASIC (application specific integrated circuit) device (12 mm^2)(14). These design tools are becoming applicable for actual devices.

Control of Systematic Defects

As discussed above, systematic defects should be removed at the design stage. However, variations of process parameters, which can not be dealt with in manufacturability verification, may induce systematic defects at the manufacturing stage. For example, lens aberration and optical elements errors of exposure tools may affect the generation of systematic defects(15). Application of different tools causes systematic defects although the current tools do not.

To prevent these defects, detection and removal of all "potential" systematic defects at the design stage is necessary. Verification of manufacturability for larger process windows in terms of exposure dose and focus, or for actual tool performance data is required.

Monitoring "potential" systematic defects at the manufacturing stage is also necessary, and accurate measurement technology of two- or three-dimensional pattern shape is important. Such information can be used for fixing process conditions and adjusting them through APC (advanced process control).

Future Prospects

It is becoming more important to improve accuracy of model for manufacturing verification and OPC to remove systematic defects. Measuring actual mask

pattern shapes is discussed to improve simulation accuracy, where the ideal shape is supposed for mask in the past(16). For manufacturing technology, it is indispensable to reduce tool matching and lens aberration further, and to control the process more stringently.

For the double patterning technology we briefly described before, new issues such as pattern split, pattern reconnection, and strict overlay control need to be investigated.

Other DFM activities than lithography are also considered.

(1) DFM for random defects(17): Optimization of line and space widths in terms of yield and chip area through CAA (critical area analysis)

(2) Electrical DFM(18): Circuit verification after the correction and modification of circuits characteristics considering actual two- or three-dimensional pattern shapes

(3) Model-based dummy pattern generation(17): Optimal dummy pattern generation and insertion to improve process related variations such as planarity in CMP (chemical-mechanical polishing) process and uniformity of RTA (rapid thermal annealing).

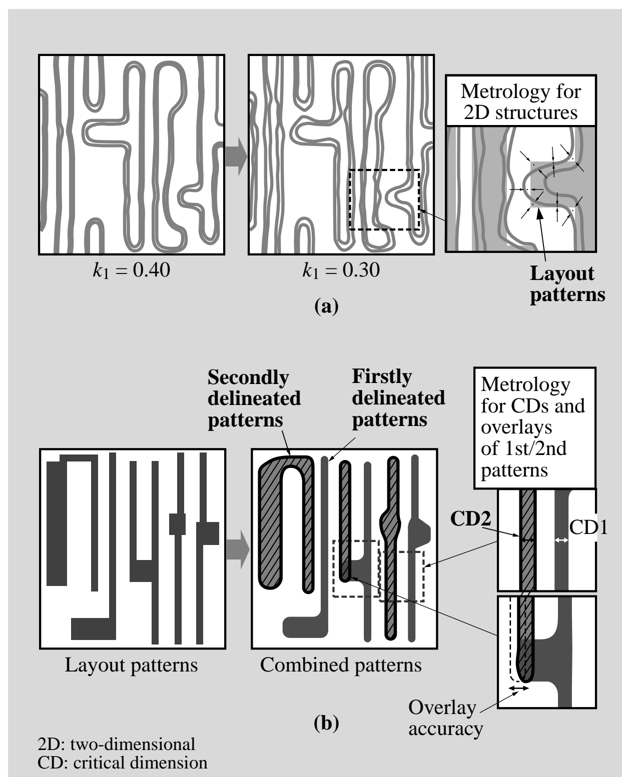

Fig. 9—Issues of Future Metrology.
Example of two-dimensional metrology (a) and example of metrology for double patterning (b) are shown.

ROLE AND REQUIREMENTS OF METROLOGY TECHNOLOGY

Improvement in metrology accuracy is indispensable for improving manufacturability and OPC verification because the required accuracy is in the order of 1 nm. The technology of two- or three-dimensional shape measurement is important for monitoring systematic defects, improving accuracy of OPC/verification models, and measuring mask pattern shapes. It is also important to simplify the recipe generation tasks to meet increasing demands of the increase in the number of measurement points.

Metrology technology thus plays an important role in low-k_1 lithography, and it mediates between the design and lithography worlds with EDA tools in the DFM scheme.

For the double patterning technology, it is necessary to measure the CD (critical dimension) and overlay very accurately for both firstly and secondly delineated patterns. The requirement of overlay for double patterning technology is considered to be less than 3 nm, and stringent precision and accuracy is required for metrology(19). These new issues related to metrology are summarized in Fig. 9.

CONCLUSIONS

We have reviewed the issues optical lithography is now facing, and the design strategy to overcome those issues. We have also discussed the current status and issues of DFM, and the role and requirements of metrology technology.

To fabricate semiconductor devices below the 45-nm technology node, we have to pursue low-k_1 lithography, where removal of systematic defects and DFM are key technologies. Design and lithography technologies can not be considered separately, and metrology technology plays an important role.

DFM has just been put to practical use, and its accuracy needs to continuously improve. The requirement for metrology is changing from one-dimensional to two-or three-dimensional measurements. It is important to cope with new requirements along with further improvements on accuracy.

We anticipate new issues associated with double patterning technology which is supposed to bridge to EUV lithography. We should be aware of the trend in lithography as a key technology of miniaturization, and address new requirements for metrology technology. We will continuously pursue research and development of metrology technology and its application.

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